

# Characterization of SOI Wafers by Photoluminescence Spectroscopy, Decay and Micro/Macro-Mapping

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Silicon-on-insulator (SOI) wafers are entering mainstream LSI production, since the SOI structure overcomes the limits of speed and power consumption of conventional MOSFET devices. An ultrathin top Si layer with a thickness around 0.05 - 0.2  $\mu\text{m}$  is required for these devices and has been realized by sophisticated techniques, such as SIMOX (separation by implanted oxygen), Smart-Cut<sup>®</sup> and ELTRAN<sup>®</sup>(epitaxial layer transfer). Since the crystalline and interfacial quality of the top Si layer directly affects the device performance and yield, accurate characterization of the layer is one of the biggest issues in SOI devices. In this paper the author reviews the characterization of SOI wafers by photoluminescence (PL) [1-4].

We have focused on an electron-hole condensation phenomenon inherent in the SOI structure under UV light excitation. The shallow penetration depth of the UV light and the confinement effect of photo-excited carriers in the SOI structure induce a characteristic condensate luminescence from the top Si layer, known as electron-hole droplet (EHD) luminescence at cryogenic temperatures. The intensity and decay time of the luminescence reflect the crystalline and interfacial defects. The detection of deep-level PL allows us to identify the origin of defects in a straightforward manner. PL under UV light excitation combined with PL under visible and near infrared (NIR) light excitation is quite effective for use in analyzing the defects located in the top Si layer, in the region close to the interface, and in the substrate.

PL spectroscopy was performed on SOI wafers at 4.2 - 300 K under various cw laser excitations ranging from deep UV (266 nm) to NIR (1064 nm). The intensity mapping of specific spectral components was done at room temperature on a full wafer up to 300 mm in diameter, and microscopic mapping of a particular region of interest was also performed under a resolution as high as 1  $\mu\text{m}$ . Decay time of the EHD luminescence from SOI wafers at 4.2 K was measured under a pulsed UV laser (266 nm) excitation.

We investigated the annealing behavior of defects in SIMOX wafers with  $\text{O}^+$  doses of 2, 4, 6  $\times 10^{17} \text{cm}^{-2}$ . The wafers were subjected to isochronal annealing at temperatures from 800 to 1350 $^{\circ}\text{C}$  [2], and generation and annihilation of deep-level PL associated with interstitial-type {311} defects and dislocations were clearly observed depending on the annealing stage. The EHD luminescence dominated the spectrum after annealing at 1350 $^{\circ}\text{C}$ . These findings agreed with the TEM (transmission electron microscopy) observation.

The EHD luminescence decay was shown to reflect the crystalline and interfacial quality of SOI wafers [3]. Comparison of the decay among SOI wafers fabricated by various techniques is shown in Fig. 1. Although there were no differences in spectral shape among the wafers, the decay time varied from one wafer to another. We believe that the rapid decay originates from the poor quality of the top Si layer and the interface between this layer and the buried oxide layer.

Mappings of the band-edge emission from state-of-the-art 200 mm SOI wafers fabricated by three different techniques are shown in Fig. 2, where upper figures are PL on the top Si layers obtained under UV excitation and lower figures that on the substrates under visible excitation. Characteristic nonuniform patterns peculiar to respective fabrication methods were observed in full wafer mapping. We also discovered a micron-sized irregularity in the top Si layer of some SOI wafers [4].

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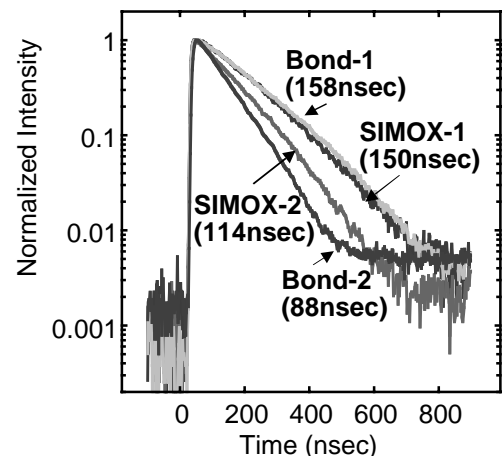


Fig. 1. Comparison of decay time of the EHD luminescence in various SOI wafers with  $t_{\text{SOI}} = 170 - 200 \text{ nm}$  at 4.2 K.

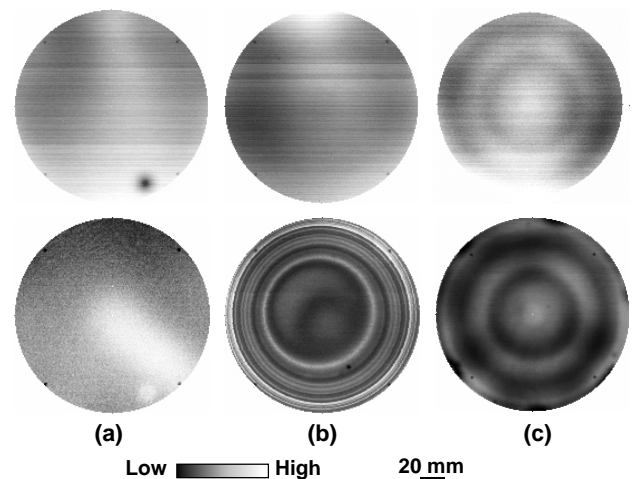


Fig. 2. PL mapping on (a) SIMOX, (b) Unibond<sup>®</sup>, and (c) ELTRAN<sup>®</sup> wafers with  $t_{\text{SOI}} = 170 - 200 \text{ nm}$  at room temperature: Upper and lower figures are on top Si layers and substrates, respectively.