**Fully Integrated Plasma-Activated Bonding (PAB) for High Volume SOI Substrate Manufacturing Process**

Igor J. Malik, Sien Kang, Jim Sullivan, Martin Fuerfanger, Philip J. Ong, and Francois J. Henley

Silicon Genesis Corporation (SiGen)
61 Daggett Drive
San Jose, CA, USA

The quality, availability, and pricing of SOI wafers will determine the speed of their adoption as starting substrates for mainstream integrated device manufacturing. While substrate availability is a commercial issue and will not be dealt with in this paper, quality and pricing directly depend on the manufacturing process. We are going to review the SiGen layer-transfer process with the emphasis on Plasma-Activated Bonding (PAB), room temperature cleaving, and non-contact surface finishing. We will demonstrate superior performance on key quality parameters (SOI thickness uniformity, HF defects, etc.) for 200 mm diameter SOI wafers. The scalability of the SiGen process is demonstrated on data from 300 mm diameter ultrathin (UT) SOI wafers. The range of SOI specifications (SOI layer thickness: tSOI, buried oxide thickness: tBOX) achievable with the SiGen layer-transfer process is reviewed. SiGen's manufacturing processes with PAB and room temperature cleaving are uniquely suited to a variety of applications from microprocessors and MEMS to multi-stack optoelectronics.

The process flow for the SiGen SOI substrate manufacturing process includes four key steps (a-d):

**a**. Cleave-plane formation – implant or epi: SiGen developed two methods for cleave plane formation: one using implantation of hydrogen [1], the other using an epitaxially grown strained SiGe layer [2].
**b**. Bonding -PAB: Prior to bonding, the clean surfaces are activated in a low-energy plasma; we refer to this sequence as fully integrated plasma-activated bonding (PAB)[3]. The plasma treatment causes the initial bond strength to be significantly larger relative to wet bonding. The PAB process uses different conditions for Si (hydrophilic) to $SiO_2$ bonding vs. $SiO_2$ to $SiO_2$ bonding. The PAB process has been proven on other than Si-based materials as well. The key requirement for a low-defect level bonding process is a strict contamination control; this condition is assured by wafer cleaning immediately prior to bonding and a mini-environment containing both the plasma activation and the bonding chamber.
**c**. Cleaving -CCP: The layer transfer is performed in a controlled cleave process (CCP) tool. One major advantage of this step is that it is performed at room temperature, therefore enabling applications with severe thermal budget constraints. Another advantage is the smoother as-cleaved surface compared to thermal cleaving methods.
**d**. Surface finishing – ES/ET: The surface roughness is reduced to sub-angstrom levels by the epi smoothing (ES) process. This step is performed in an epitaxial reactor by vapor HCl etch [4]. It is also possible to add to the as-cleaved device layer thickness through an epi-thickening (ET) process. This ES/ ET capability enables the manufacture of a wide SOI specification spectrum (tSOI from <20 nm to >5 micron).

Fig. 1 shows a recent 200 mm ultrathin (UT) SOI wafer demonstrating the potential for sub-nm control of the non-uniformity (range = max-min). Similar performance (range = 2.3 nm) was demonstrated on a 300 mm UT-SOI wafer with the same target device layer thickness (tSOI = 50 nm).

Advanced SOI devices using fully-depleted SOI substrates [5] require the minimization of device layer non-uniformity on a wide range of lateral scales – from the macro-scale wafer level (see Fig. 1) to the atomic level: Fig. 2 shows low surface roughness (which can be considered micro-scale layer non-uniformity) from AFM scan sizes from 2x2 micron to 50x50 micron on a 300 mm UT-SOI wafer.

References:
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[**3**] S Farrens, JR Dekker, JK Smith, and BE Roberds: "Chemical Free Room Temp. Wafer to Wafer Direct Bonding", J Electrochem. Soc., **142** (11), p. 3950, 1995.
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[**5**] R Chau, B Doyle, J Kavalieros, D Barlage, A Murthy, M Doczy, R Arghavani, S. Datta: "Advanced Depleted-Substrate Transistors: Single-gate, Double-gate and Tri-gate", p. 68, SSDM, Nagoya, Sept. 2002.

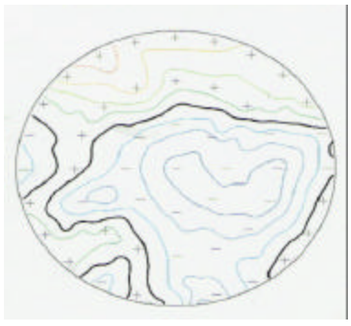

Fig. 1: A 200 mm UT-SOI wafer with average tSOI=50.1 nm and total tSOI range (max-min) of 0.8 nm (5 mm edge exclusion, 48 points)

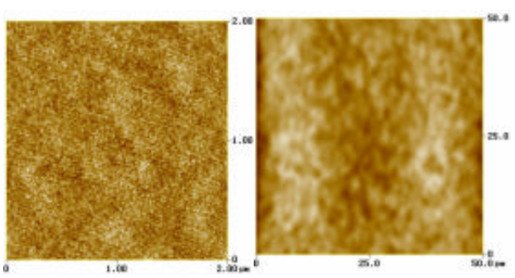


Fig. 2: AFM data – surface roughness of a 300 mm UT-SOI wafer (tSOI = 50 nm): 2x2 micron (left): rms = 0.07 nm; 50x50 micron (right): rms = 0.34 nm.