Advanced SOI structures based on wafer bonding : A short review

B. GHYSELEN
SOITEC - Parc technologique des Fontaines - 38190 Bernin, France

Bonded Silicon On Insulator (SOI) wafers, such as those made by SOITEC using the Smart-Cut process are now routinely used for different industrial applications. SOI material is certainly today the first large volume demonstration that wafer bonding is a true process step that can enter into demanding mainstream applications.

While some challenges are still to be tackled for in the future (ultra-thin SOI layers in the sub 10nm range for instance [1]), those now available SOI wafers are so far somewhat simple in their structure. Indeed, in their standard commercial form, those wafers consist of blanket standard silicon material laying on standard silicon dioxide insulator.

We will present in this paper some of the on-going or future developments that will form the basis for new generations of SOI related structures. We will also see how such advanced structures put different sorts of challenges on this quite unique technological step which is direct wafer bonding.

Beyond simple silicon layer transfer

Different materials among the best candidate to enter into the realization of the new generations of SOI wafers will be considered. Among those, SiGe is an interesting case as far as wafer bonding and layer transfer is concerned. First, SiGe has been long used in combination with Si to supply an effective etch-stop system. Such selective etch system has the potential to lead to very uniform layers or to suspended structures such as membranes to be released [2,3]. SiGe will most of all be addressed here for its ability to induce strain into Si, and the well known advantages of strained Si in terms of carrier mobility and improved CMOS transistor performance [4, 5]. Strain Silicon On Insulator wafers are today envisioned as a natural and powerful suite to standard SOI and/or bulk-like strained Si layers [6, 7]. We will show how the Smart-Cut process can be advantageously applied to the realization of such structures. Of particular importance is the characterization of how a wafer bonded interface can handle strain in adjacent layers. Fig 1 shows an example of Strained Si on insulator structure that will be of interest in this paper.

Beyond SiO2 bonding layers

Other non silicon based materials will be considered too, as well as other specific materials, for the formation of buried layers (Si_3N_4 [8] etc ..).

Patterned layer transfers

SOI-like patterned layers will be addressed too. Indeed, such heterogeneous structures may find a broad set of applications, ranging from double gate architectures [9] to System On Chip architectures combining at least two different technologies among Fully depleted SOI, partially depleted SOI or bulk Si technologies [10, 11, 12].

Multiple layer transfer

Multiple stacks [13] realized by multiple layer transfers based on wafer bonding will also be considered as a tool to more complex structures.

In each case, we will emphasize on showing how wafer bonding is key in the successful completion of the advanced wafer bonded structures investigated. Some cases will be illustrated through examples of achievements performed at SOITEC, in collaboration with LETI [14].

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Figure 1 : Strained Silicon On insulator structure based on SiGe layer transfer.

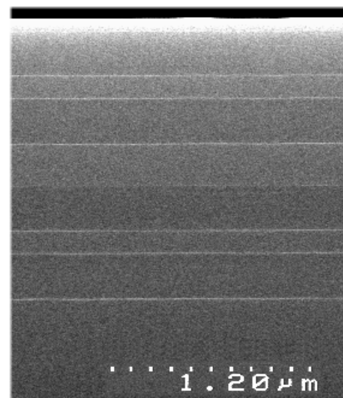

Figure 2: Multiple SOI realized by multi layer transfer.