Wafer Bonded Abrupt Junction Tunnel Diodes

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Wafer bonding is an enabling technology that allows the fabrication of a variety of complicated structures that would be difficult or impossible to make by other means. The process of hydrophobic bonding removes the thin native oxide at surface of silicon wafers. For devices that utilize bulk conduction through the bond interface, this native oxide would reduce or destroy performance by creating traps and electrical discontinuities that will affect the I-V and C-V characteristics at the interface [1].

Wafer bonding has been used to fabricate several important high power devices such as silicon controlled rectifiers and double sided insulated gate bipolar devices [2]. Another useful device for power applications is a stacked diode. In this structure, multiple diodes are stacked in series using wafer-bonding techniques to provide a device with very high reverse blocking voltage.

Between each diode of a stacked diode structure (PN/PN/PN) is an interface diode of the reverse orientation (P/NP/NP/N). In order for the stacked diode structure to have low forward voltage drop, the interface diodes must be tunnel or backward diodes with minimum reverse voltage drop for high current performance. An important step in fabricating a stacked diode structure is design and optimization of the interfacial tunnel diodes.

Tunnel diodes were fabricated by direct hydrophobic bonding of a highly doped p-type wafer to a highly doped n-type wafer. The wafers were 125mm diameter (001) silicon. Net doping was on the order of $1x10^{21}/cm^3$ for both n and p type wafers at the wafer surface with bulk doping of approximately $1x10^{19}$. The wafers were thinned to approximately 200μm each before bonding and implanted on the backsides for good ohmic contact.

An annealing study was performed to optimize the process for reduced interfacial voids, maximum diode performance, and produce sufficient bond strength to allow wafer dicing. Initially, a high temperature rapid thermal anneal was thought to produce void free bonds, however after acoustic microscopy inspection, the rapid thermal processing produced a high density of very small voids. It was found that, at a minimum, a furnace anneal of 400°C was required for sufficient bond strength for further processing. The furnace anneal produced a few large voids which resulted in some diode structures failing during wafer dicing and further processing. Any further anneal produced a significant degradation of diode performance. Annealing above 750°C resulted in normal diode behavior.

The diodes performed linearly in reverse bias with only 40mV required to produce $100A/cm^2$ for a 0.5mm by 0.5mm diode. While these devices did show evidence of tunneling under forward bias, negative differential resistance was not observed (i.e., a current peak-to-valley ration of ~1). The large excess current was probably due to interfacial defects.

The results indicate it is possible to create tunnel diodes with high reverse current density and low voltage drop by using direct wafer bonding. This is an important step in realizing the stacked diode structure, which will result in a compact high voltage diode with low forward drop. Further development may be necessary to address interfacial voids and their effect on device reliability, performance and yield.

References:

1) O. Engstrom et. al., “Electrical Characterization of Bonding Interfaces,” J. Electrochm. Soc. v. 139, p. 3638, 1992

2) Hobart et. al “Characterization of a Bi-Directional Double-Sided Double-Gate IGBT Fabricated by Wafer Bonding” ISPSD 2001, Osaka Japan, June 4-7