Future Trends in SOI Devices

Ted R. White, Alexander Barr, Aaron Thean, Anne Vandooren, Leo Mathew, Michael Mendicino, Geoffrey Yeap, Bich-Yen Nguyen, Marius Orlowski
Motorola Digital DNA Laboratories
3501 Ed Bluestein Blvd., MD:K10
Austin, TX 78721, USA. (Tel: 512-933-7285, FAX: 512-933-2691, ted.white@motorola.com)
keywords: SOI, device trends, strained Si, FDSOI, double-gated devices, FinFET

This paper discusses the future trends of CMOS devices on SOI wafers in Motorola. Much of the early work dealt with substrate and device development on SIMOX wafers [1, 2]. This kind of work continued as bonded SOI wafers became available [3,4]. When many of the early materials and device issues had been addressed, Motorola manufactured high performance microprocessors on SOI wafers in 2001. Building microprocessors on SOI wafers provided a 15-20% increase in performance over their counterparts on bulk wafers [5].

A future trend in SOI wafers will be thinner Si layers for enhanced device performance at small technologies. While Si thicknesses have been about 1000Å at 130nm and older technologies, the thickness is expected to be around 700Å at the 90nm technology node. A 15-20% improvement in ring oscillator delay is seen by this decrease (Fig. 1). PDSOI requires body-contacted devices to suppress floating body effect. A novel body contact structure was proposed to provide a simple means of eliminating the floating body effect with no impact on performance and minimal added cost [6].

At the 65nm node strained Si devices will be introduced [7]. Silicon Germanium On Insulator SGOI provides high performance through enhanced mobility devices in a thin strained Si layer on relaxed SiGe [8]. We observed extremely high electron mobility enhancements in strained Si devices on bulk wafers (Fig. 2). Given this enhancement on bulk, simulations of devices on SGOI show performance surpassing ITRS high performance and low operating power targets for a physical gate length of 30nm (Fig.3). As the top Si/SiGe layers continue to thin, eventually there will be no room for the SiGe. Another structure, Strained Si On Insulator (SSOI), where the SiGe is removed, may be ready then [9]. At this point, PDSOI devices should be approaching fully depleted (FD) operation.

FDSOI and FDSSOI will be used to overcome scaling issues associated with conventional PDSOI devices for high performance and low power, respectively. While FDSSOI substrates are not readily available yet, Motorola has a long history of FDSOI device development with advanced features such as metal gate electrodes [10, 11, 12], elevated extensions [13], and high k gate dielectrics [14]. Simulations of FDSOI devices show that they surpass the ITRS low operating power targets for a physical gate length of 30nm and a Si thickness less than about 3nm (Fig. 4). FDSOI devices are desirable for low-power, low-voltage applications due to low junction capacitance. In addition, this technology can provide improved subthreshold slope, is free from floating body effects, has reduced sensitivity to temperature and Single-Event Upset, and larger immunity to short channel effects. However, several substrate issues remain for ultra-thin SOI. These include short- and long-range non-uniformities, and high densities of pinholes in the Si layer (Fig. 5, 6) [15].

Ultimately, scaling issues will drive the conversion to double-gated devices. Our early work on FinFETs (Fig. 7) is encouraging [16]. SOI wafers provide a convenient substrate for processing these devices providing all the advantages of FDSOI devices.

The strengths and weaknesses of the three novel devices can easily be seen in saturated I_D-V_G curves (Fig. 8). Strained Si devices (SGOI, SSOI, and strained DGFETs) with their enhanced mobilities, I_{on}, and I_{off} should meet high performance targets. FDSOI and FinFETs with their extremely low I_{off} and subthreshold slopes should meet the low power targets. Minimization of parasitic resistances will determine the performance level achieved with these devices. The combination of novel structures and SOI substrates will enhance the continued following of Moore's Law into the near future.

References

[1] M. E. Burnham and S. R. Wilson, "An overview of SOI by implantation of oxygen: materials, devices and circuits," Proceedings of the SPIE - The International Society for Optical Engineering, vol.530, 1985, pp.240-50.
[2] J. D. Whitfield, et. al., "An electrical characterization of SOI films using devices formed by oxygen implant and rapid thermal processing," Rapid Thermal Processing of Electronic Materials. Symposium, 1987, pp.241-6.
[3] S. R. Wilson, et. al., "Materials, device and gate oxide integrity evaluation of SIMOX and bonded SOI wafers," IEEE SOI Conf., 1995, pp.143-5.
[4] D. T. Pham, et al, "SOI materials defect characterization," IEEE SOI Conf., 1997, pp.144-5.
[5] M. Mendicino, "SOI Technology for MPU Applications," Ext. Abst. SSDM Conf., 2001, pp. 256-7.
[6] B. W. Min and M. Mendicino, "Effective body contact in SOI devices by partial trench isolated body-tied (PTIBT) structure," Semiconductor Device Research Symposium, 2001, pp. 469 –472.
[7] G. G. Shahidi, "Oxide isolation ramps next-generation process," EE Times, September 23, 2002.
[8] T. Mizuno, et. al., "High performance CMOS operation of strained-SOI MOSFETs using thin film SiGe-on-insulator substrate," Symp. On VLSI Technology, 2002, pp. 106 –107.
[9] T. A. Langdo, et. al., "Preparation of novel SiGe-free strained Si on insulator substrates," IEEE SOI Conf., 2002, pp. 211-12.
[10] B. Maiti et al., "PVD TiN metal gate MOSFETs on bulk silicon and fully depleted silicon-on-insulator (FDSOI) substrates for deep sub-quarter micron CMOS technology," in Tech. Dig. IEDM, 1998, pp. 781-784.
[11] J. Chen et al., "0.18 um metal gate fully-depleted SOI MOSFETs for advanced CMOS applications," Symp. On VLSI Technology, 1999, pp.25-26.
[12] B. Cheng, et. al., "Metal gates for advanced sub-80-nm SOI CMOS technology," IEEE SOI Conf., 2001, pp.91-2.
[13] S. Bagchi et al., "Fully depleted SOI devices with TiN gate and elevated source-drain structures," IEEE SOI Conf., 2000, pp.56-57.
[14] A. Vandooren, et. al., "Ultra-thin body fully-depleted SOI devices with metal gate (TaSiN) gate, high K (HfO_2) dielectric and elevated source/drain extensions," IEEE SOI Conf., 2002, pp. 205 –206.
[15] A. Vandooren, et. al., "Scaling assessment of fully-depleted sot technology at the 30nm gate length generation," IEEE SOI Conf., 2002, pp. 25 –27.
[16] L. Mathew, et. al., "Vertical CMOS Double Gate

MOSFET with notched poly gates," Proc. Silicon Nanoelectronics Workshop, 2002, pp. 5-6.

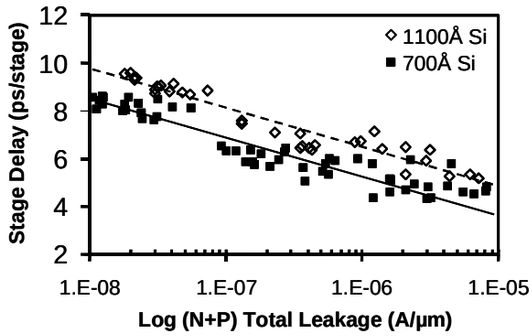

Figure 1. Inverter stage delay as a function of leakage at 1.3V with a fan out of 1 for two Si thicknesses.

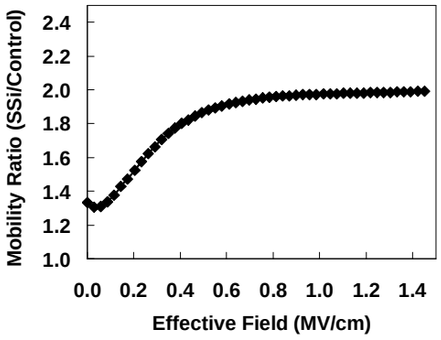

Figure 2. Mobility enhancement for identically processed strained Si and Si NMOS devices on bulk Si as a function of effective field. The transistors were 10x10µm with a drain voltage of 0.1V.

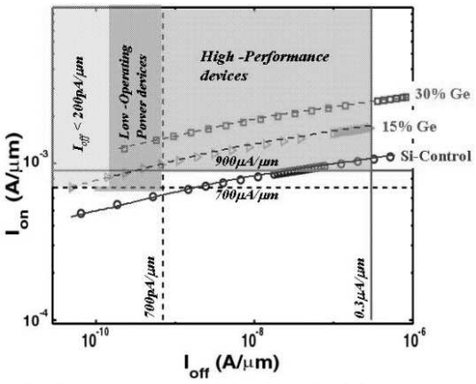

Figure 3. Simulated I_{on} and I_{off} for NMOS devices with physical channel lengths of 32nm and a drain voltage of 0.9V.

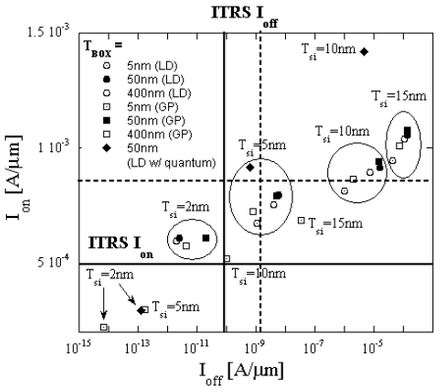

Figure 4. Simulated I_{on} and I_{off} of FDSOI devices for various Si and BOX thicknesses. The physical channel length is 30nm and the drain voltage is 1V.

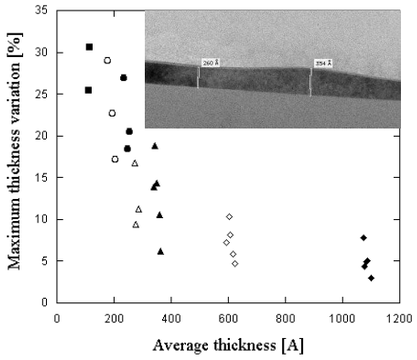

Figure 5. Short- and long-range Si thickness variations of bonded SOI wafers as a function of Si thickness after successive oxidations and etches.

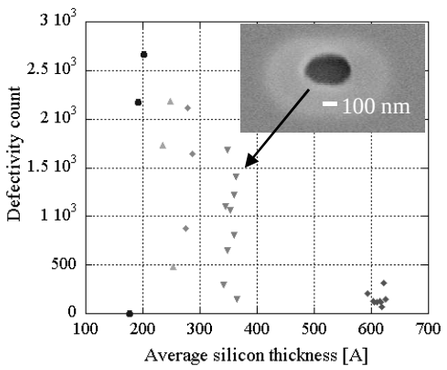

Figure 6. Defects count versus average silicon film thickness after successive oxidations and etches. Defect size detection limit was 0.15µm.

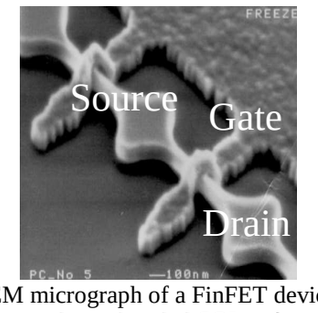

Figure 7. SEM micrograph of a FinFET device after gate poly etch processed on a bonded SOI wafer.

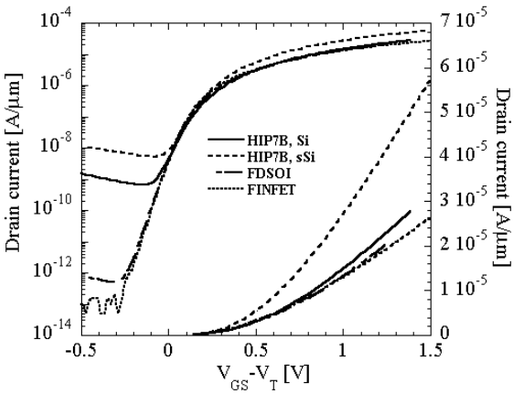

Figure 8. Linear and Log I_D-V_G-V_T curves Si on bulk, Strained Si on bulk, FDSOI and FinFET NMOS devices. The devices were normalized to 10x10µm and a scaled linear V_T at 100nA/µm with a drain voltage of 1.5V.