Fabrication and characterisation of multi-layered SOI for MEMS applications

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Fusion bonded silicon on insulator (SOI) has become an important substrate for fabricating advanced electronic devices, and micro-electro-mechanical system (MEMS) or optical MEMS (MOEMS) structures. These substrates are manufactured at Analog Devices Belfast, where we have also developed MultiBond™ which is a multiple layer (triple and above) SOI wafer fabricated using fusion bonding, containing interfacial layers of oxide and other materials. Both patterned single crystalline silicon and patterned intermediate layers can be incorporated. This approach enables the fabrication of structures containing micro-machined and trench isolated integrated electronic devices in the same die. A variety of products, such as R.F switches, accelerometers, pressure sensors, optical switches, actuated mirrors and wave guides can be made using this type of wafer. The MultiBond™ SOI gives greater ease and flexibility in the manufacture of MEMS and MOEMS components compared to single SOI layers. In this work, we have investigated the bonding ability, thickness uniformity and stress levels in the multi-layered wafers.

Six inch diameter wafers were used for the investigation. The experiments were designed to compare different bonding processes, as well as the effect on stress in 3-stack and 4-stack samples of including different types of intermediate layer material. We found that high quality bonding can be achieved with good thickness control, independent of the fabrication method used. The stress in the overall structure is found to be controlled by the balance between the combined stresses at the oxide silicon interfaces of the SOI buried oxide layers and that exerted by the oxide on the back surface of the handle wafer. The influence of the interfacial layers on crystal defect generation in the SOI will also be reported.

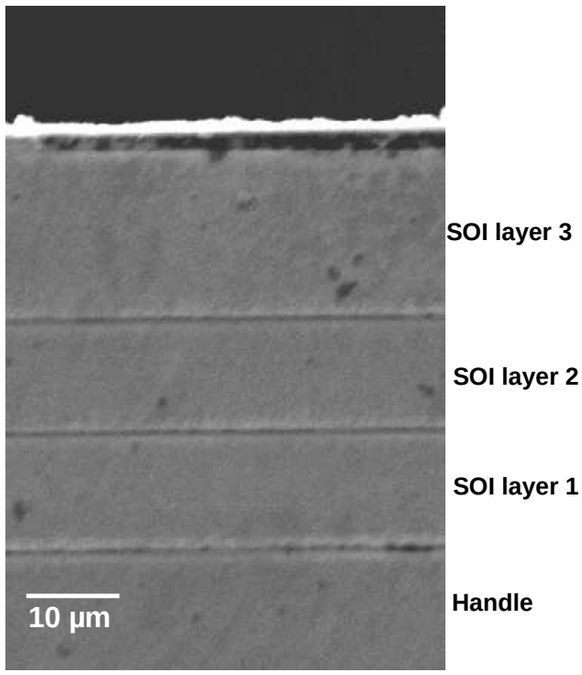

Figure 1. Cross-sectional SEM image of a 4-stack SOI wafer.

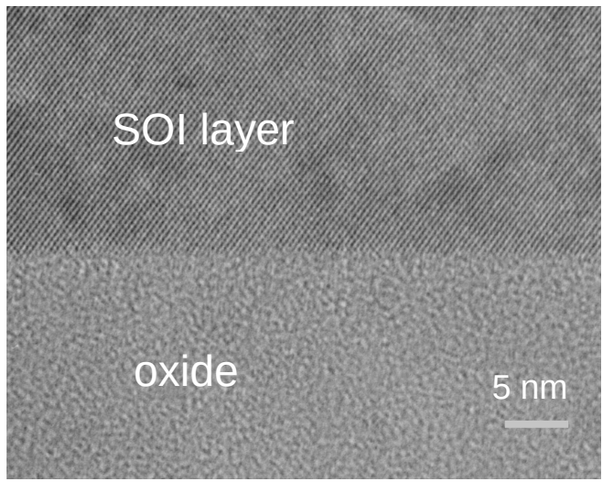

Figure 2. Cross-sectional TEM image of the bonded interface of an SOI wafer.