Bonding and contacting of MEMS-structures on wafer level

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Joining technologies like the seal glass wafer bonding are effective and cost favorable procedures for hermetically encapsulation of MEMS-structures on wafer level also in connection with electronic structures. The advantages of this procedure are a simple process control, the low demands on quality of the substrate surface (roughness and purity) and the possibility of bonding of a wide range of applicable materials, which can be used as bonding surfaces. A suitable approach for the patterned deposition of the glass paste on the substrates is screen printing. Essential emphasizes of such technology developments are the fabrication of a screen for substrates joining together, which is matched to the structure layout, and the optimization of the print process itself. The screen design has to be optimized regarding to dimensions, which can be realized on one screen in dependence on the absolute structure dimensions like bond frame wide and material thickness. Additional suitable print parameters for glass materials like squeegee pressure, squeegee velocity and the off-contact distance have to be detected. The paper presents print results of 100 µm to 150 µm wide bond frames with a material thickness of about 15µm (after sealing, see Fig. 1) which were realized by suitable print process control. The developed bonding process using this parameters led to hermetic sealed MEMS structures. Within the paper the parameters of the print and bonding process will be presented and the print process limits and possible sources of errors will be demonstrated by means of print and bonding results. The applicability of this wafer bonding technique will be shown by fabrication of hermetically capped MEMS structures (see Fig. 2).

A further development during encapsulation of MEMS-structures is the production of gas-proof, electric feed-throughs, which either can be implemented at the bond interface, through the active part of the structures or through the cap wafer. Two possible variants were examined. The first variant is based on aluminum conductor paths embedded in CVD-oxide and -nitrite layers. Goal of this development was to fabricate bondable surfaces above the buried conductor paths, which are also suited for the direct silicon bonding. This was achieved by CMP (Chemical Mechanical Polishing) of deposited masking layers over the aluminum. In a second variant the conductor paths were directly covered with a glass paste during a screen printing process (see Fig. 3). It could be shown for different dimensions that a gas-proof seal can be produced using this procedure.

The results of our investigations regarding integration on the wafer level showed, that it is possible to encapsulate MEMS-structures on wafer level by means of seal glass bonding and electrical contacting (see Fig 4). Continued developments will be performed with the goal of integration of MEMS-structures with electronic structures on wafer level.

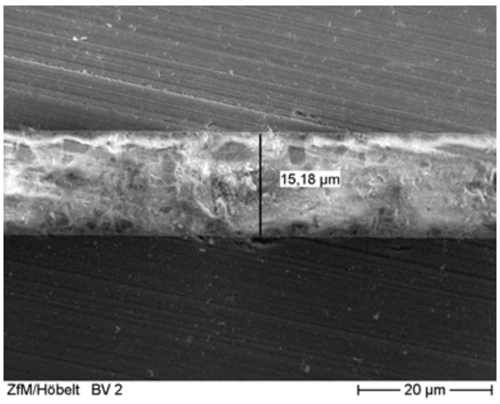

Fig. 1: Glass paste after the bonding of two silicon substrates

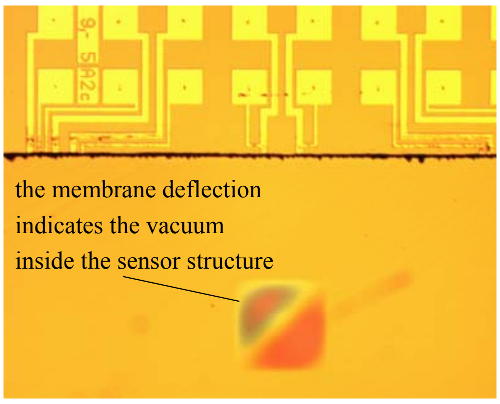
the membrane deflection
indicates the vacuum
inside the sensor structure

Fig.2: Hermetic sealed MEMS structure with wire bond pads

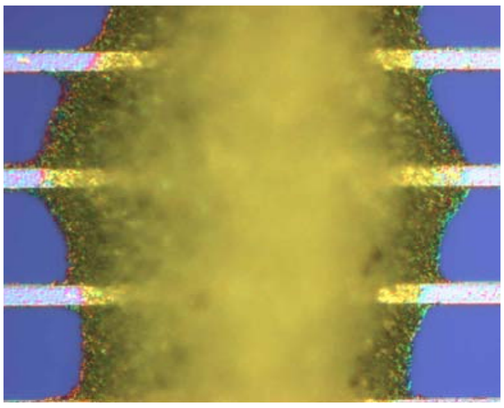

Fig.3: Printed glass paste over conductor paths

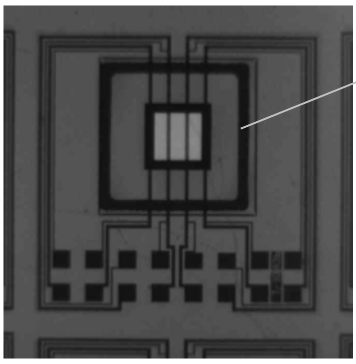
Glass brond frame
printed over
conductor paths
(bond frame wide
250µm)

Fig. 4: Capped MEMS structure with electrical feed-throughs