Traps at the bonded Si/SiO_2 interface in silicon-on-insulator structures

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The results of Charge Deep Level Transient Spectroscopy (Q-DLTS) study of Si/SiO_2 interfaces in semiconductor-on-insulator (SOI) structures are presented. Two type of SOI were investigated: (1) SOI fabricated by wafer bonding and hydrogen slicing and (2) SOI fabricated by wafer bonding and chemical - mechanical thinning of one of the bonded wafers (back-etch SOI, BESOI). We have demonstrated recently [1], that spectrum of traps at the bonded Si/SiO_2 interface is differed from that for traps in Si/SiO_2 interface prepared by thermal oxidation: The trap energies for the bonded Si/SiO_2 interface are localized in the range from $E_C - 0.17$ to $E_C - 0.37$ eV. The lack of the transient SiO_x layer at the bonded interface is suggested to lead to a relatively narrow interval of trap energies. Thermal treatments of SOI structures at a temperature of 430°C in hydrogen ambient lead to transformation of traps at the bonded Si/SiO_2 interface. The energy spectrum of the observed traps shifts from the initial energy interval of $E_c - (0.17\text{-}0.37)$ eV to an energy interval of $E_c - (0.08–0.22)$ eV (Fig.1). The density of these traps is slightly increased with annealing time. Treatments in hydrogen ambient at higher temperatures (≥ 550°C) lead to generation of traps at the bonded interface with a continuous energy spectrum and widely ranging capture cross sections according to DLTS data. The energy distribution of interface states of BESOI is familiar to that of SOI, but the density of states is about one order higher (Fig. 2). Hydrogen presented in SOI during fabrication process (technology of hydrogen slicing) was found to partially neutralize the traps at the Si/thermal SiO_2 interface. Obtained results allow us to state that the traps localized at the bonded Si/SiO_2 interface of SOI structures have a different origin compared to traps localized at the conventional Si/SiO_2 interface fabricated by thermal oxidation. It can be speculated that some extended defects located right at the bonded interface can be formed during the bonding procedure to compensate for the lattice mismatch. The origin of traps at the bonded interface is discussed in the report.

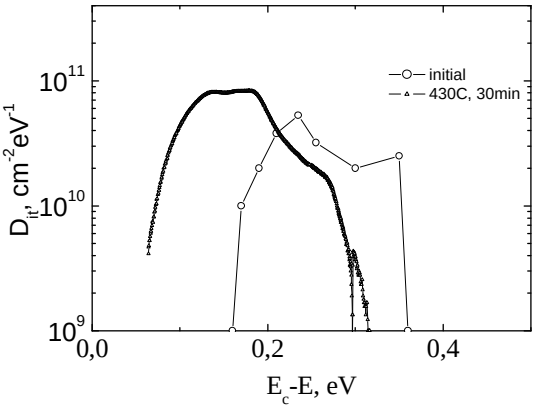

Fig. 1. Distribution of interface states at the bonded interface (top silicon layer / buried oxide interface) of the SOI structures before and after annealing in hydrogen ambient at temperature 430°C during 30 min.

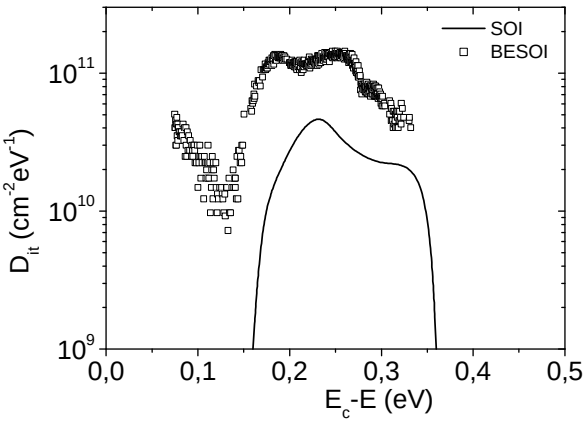

Fig. 2. Distribution of interface states at the bonded interface top silicon layer / buried oxide interface of SOI structures fabricated by wafer bonding and hydrogen slicing and BESOI.

References

[1] I.V.Antonova, O.V.Naumova, J.Stano, D.V.Nikolaev, V.P.Popov, V.A.Skuratov, Appl. Phys. Lett., **79**, 4539 (2001).