

## RECENT RESULTS OF STACK DEVELOPMENT AT FORSCHUNGSZENTRUM JÜLICH

R. Steinberger-Wilckens<sup>1</sup>, L.G.J. de Haart<sup>2</sup>,  
I.C. Vinke<sup>2</sup>, L. Blum<sup>2</sup>, A. Cramer<sup>3</sup>, J. Remmel<sup>3</sup>,  
G. Blaß<sup>2</sup>, F. Tietz<sup>2</sup>, W.J. Quadackers<sup>2</sup>

(<sup>1</sup>) Project Management Fuel Cells, (<sup>2</sup>) Institute for  
Materials and Processes in Energy Systems,  
(<sup>3</sup>) Central Department of Technology

Forschungszentrum Jülich, D-52425 Jülich, Germany

Since the mid-nineties several generations of SOFC stacks have been designed and tested incorporating the anode substrate-type cells developed in Jülich. The 5<sup>th</sup> generation, the so-called E-design stacks, with metallic interconnect constitutes the 'work horse' used for testing materials, cells and manufacturing processes in cell and stack development since its introduction in the year 2000 (1). A 40-layer stack (40 cells of 20 x 20 cm<sup>2</sup>), manufactured according to the E-design, was put into operation in mid-April 2002. All ferritic parts were made of the commercial steel type 1.4742. The stack delivered 9.2 kW<sub>el</sub> in operation with hydrogen and 5.4 kW<sub>el</sub> with methane as fuel (2). Whilst a small fraction of hydrogen was added to simulate pre-reformed natural gas, the stack nevertheless operated at approx. 100% internal reforming. The stack was run with a constant current density of 0.5 A/cm<sup>2</sup> for the first 1000 h of continuous operation (see Fig. 1). After a reduction of the furnace temperature the stack continued to operate in thermal self-sustaining mode, still producing between 4.0 and 4.5 kW<sub>el</sub> with methane as fuel. Current density was lowered to 0.3 A/cm<sup>2</sup> after 1000 h, until it was switched off after a total of approx. 1250 h. Average degradation was in the range of 10%/1000 h at an average temperature below 850 °C, typical for the unprotected ferritic steel 1.4742.

A series of E-design short-stacks (2 cells 10 x 10 cm<sup>2</sup>) was assembled with interconnects manufactured from a modified ferritic steel coded JS-3 (1,3). The ceramic cathode contact layer LCC2 was developed for this type of interconnect (1,4). Fig. 2 shows the time dependence of one of these short-stacks during operation with hydrogen at 0.3 A/cm<sup>2</sup> and 800 °C. The stack was operated over 4000 h with a degradation rate for both cells between 2 and 3%/1000 h.

A further short-stack, also with JS-3 interconnects, was subjected to a total of 40 thermal cycles after an initial period of 1800 h of galvanostatic operation. As can be seen in Fig. 3 the degradation rate, initially also around 2-3%/1000 h, was not noticeably affected by the repeated thermal cycles.

## REFERENCES

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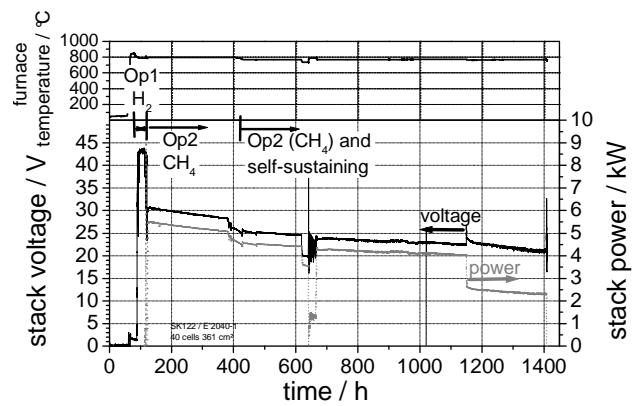


Fig. 1: Time dependence of the stack voltage and power of the 40-layer E-design stack operating on CH<sub>4</sub>/H<sub>2</sub>O, producing between 4.0 and 5.5 kW<sub>el</sub>.

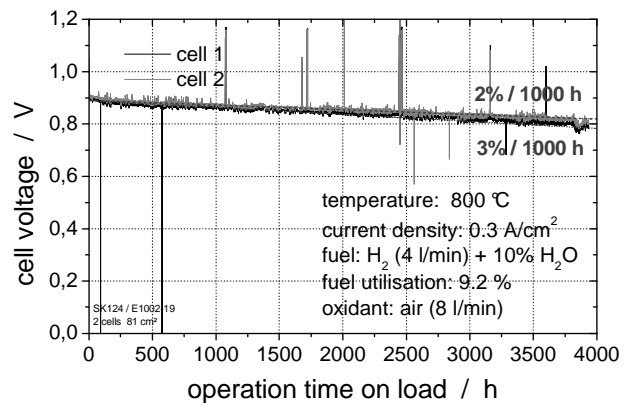


Fig. 2: Time dependence of the cell voltages in a 2-layer E-design short-stack with JS-3 interconnects during operation with H<sub>2</sub> at 800 °C and 0.3 A/cm<sup>2</sup>.

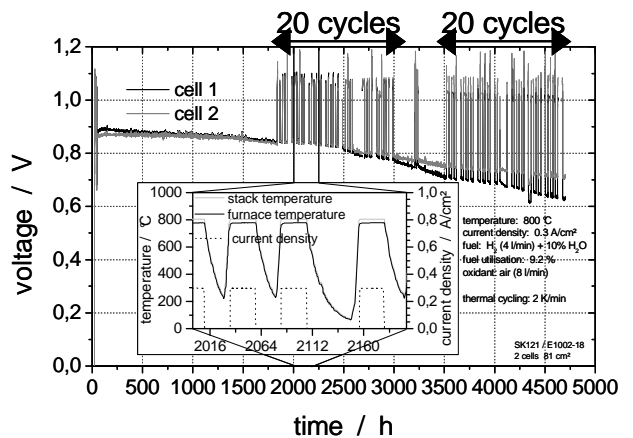


Fig. 3: Time dependence of the cell voltages in a 2-layer E-design short-stack subjected to multiple thermal cycles from 800 °C to 220 °C/75 °C.

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