UTILIZING MOCVD FOR HIGH-QUALITY ZIRCONIUM DIOXIDE GATE DIELECTRICS IN MICROELECTRONICS

S. Harasek, H.D. Wanzenboeck, W. Brezna, J. Smoliner, E. Gornik, and E. Bertagnolli
Vienna University of Technology
Institut für Festkörperelektronik
Floragasse 7, A-1040 Vienna, Austria

The increasing demands on microelectronic integrated circuits result in a steady reduction of the dimensions of the individual devices of these cicuits. Especially scaling of the gate dielectric in MOS field effect transistors (MOSFETs) has turned out to be an intriguing challenge. The need to replace thermal SiO_2 as gate dielectric with a deposited material of higher dielectric constant in future leading-edge products is current opinion. Various growth methods and post-deposition processes are currently examined in terms of achievable thin film properties. The aptitude for future integration into a production process is of prime importance in this context.

This work addresses the properties of ZrO_2 thin films on (100) silicon featuring an equivalent oxide thickness (EOT) down to 2 nm. Films are grown by MOCVD using zirconiumtetrakistrifluoroacetylacetonate ($Zr(tfacac)_4$) as precursor substance. We investigate key parameters such as chemical composition, capacitance-voltage properties, and leakage currents as well as trap and charge densities in dependence on thin film processing. Moreover, we present the effective application of the films for analytical tasks in scanning capacitance microscopy (SCM).

Fig. 1 presents the topographic evaluation of an annealed film of 15 nm thickness. The calculated roughness of the sample is R_{rms} = 1.76 Å and peak-to-peak roughness as indicated by the arrows in the line section is 5.8 Å. The staircase-like appearance of the line section is due to the height resolution limit of AFM and proves the high film smoothness. This smoothness is a key prerequisite for electronic applications, since various performance parameters of dielectric thin films may be strongly impaired by high roughness. Compositional analysis of as-grown and annealed thin films by Auger spectroscopy indicates a temperature controlled purification process almost independent of the annealing atmosphere. On the other hand, electrical characterization unveils a major impact of the annealing atmosphere on the electrical performance of the thin films in *Al-ZrO₂-p⁺Si* MOSCAPs. Annealing in oxidizing atmosphere leads to a pronounced shift of the flatband voltage (V_{FB}) in *C-V* measurements from the theoretical position towards more negative values indicating the presence of a positive oxide net charge, whereas in the case of a forming gas anneal V_{FB} almost matches the theoretical value (Fig. 2). For both types of anneal ZrO_2 provides a significant decrease in gate leakage compared to SiO_2 (Fig. 3). Again best results are obtained after annealing in forming gas and an improvement of gate leakage by more than a factor of 10^3 can be achieved for 3 nm EOT. Nanoscale characterization of the material by SCM is done in direct comparison of the behavior of SiO_2 and ZrO_2 as dielectric material in the measurements. Thus, also the scope of ZrO_2 in this scanning probe technique for two-dimensional carrier-mapping in semiconductors is assessed. The comparison proves higher stability of ZrO_2 against electrical stress, which enhances the reproducibility and reliability of the SCM measurements.

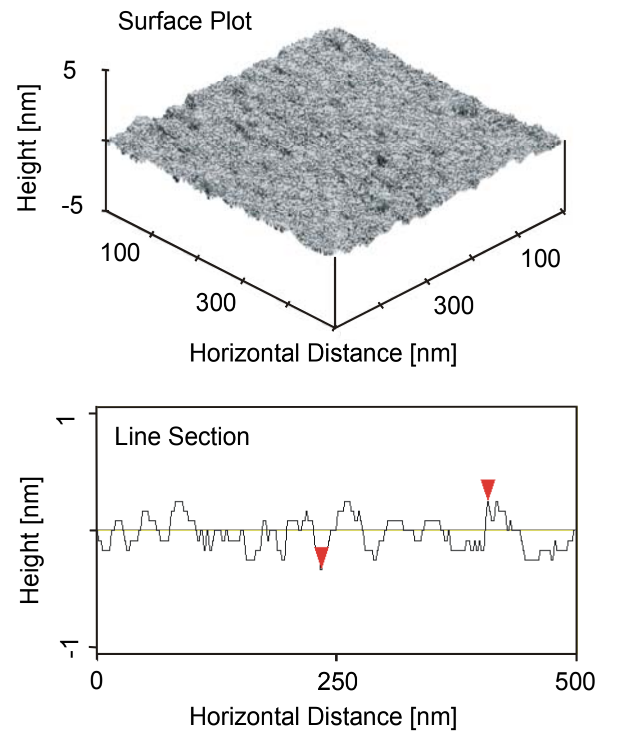

Figure 1. AFM surface plot of a 15 nm ZrO_2 thin film deposited at 450°C. A surface roughness of R_{rms} = 1.76 Å is observed with a peak-to-peak roughness of 5.8 Å in the displayed line section.

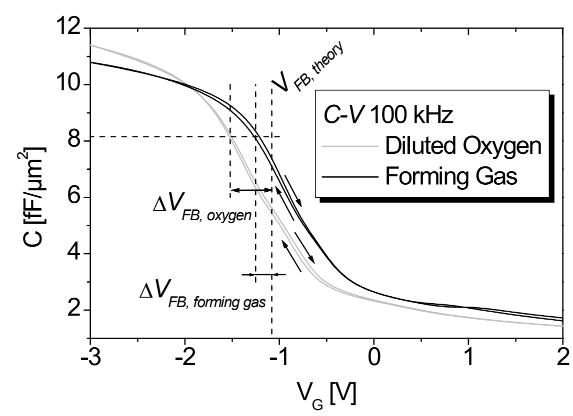

Figure 2. Well-behaved *C-V* curves after annealing in forming gas and diluted oxygen. EOT of both samples is 3.1 nm. Annealing in forming gas leads to reduced flatband shift (ΔV_{FB}).

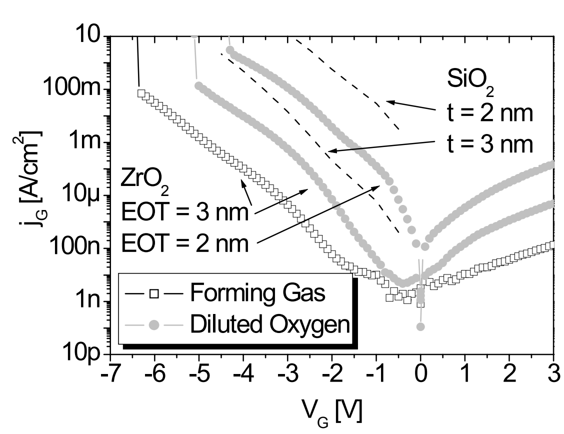

Figure 3. *I-V* characteristics of *Al-ZrO₂-p⁺Si* MOSCAPs. A more than three decades lower leakage than for SiO_2 is observed for ZrO_2 after annealing in forming gas.