Fabrication of midgap metal gates compatible with very thin SiO_2 films using low pressure chemically vapor deposited tungsten films

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Introduction: For future ULSI devices with a channel length below 0.1 µm the dopant concentration fluctuations result in large threshold voltage spreads [1], necessitating the use of undoped channels and of a gate material with Fermi level at the middle of the Si bandgap, so that it can be used for both p- and n-channel MOSFETs [2]. The use of W gates is very attractive, as W offers a work function at the Si midgap, good conductivity and compatibility with very thin gate oxide processing. Tungsten deposition by CVD using $W(CO)_6$ has been developed [3], avoiding the adhesion problems of sputter-deposited W films. In this work, MOS capacitors with W gates on thin oxides are fabricated by a process used in conjunction with copper metallization, compatible with CMOS technology, and their electrical properties are characterized.

Experimental: MOS diodes were fabricated by growing 7.5 nm thick SiO_2 films on Si wafers, using dry oxidation at 850°C, and depositing 40 nm W films directly on them by LPCVD from $W(CO)_6$ decomposition at 550°C and 0.1 Torr. After lithography and dry etching in SF_6, W gate MOS capacitors were formed. For some wafers, negative photolithography was performed after the W deposition, followed by Cu deposition by vacuum evaporation. A lift-off procedure was then carried out, yielding Cu patterns on the W film which served as masks for W dry etching. Thus, Cu/W gate devices were obtained, having W in contact with the oxide but with Cu metallization above it; in this case W served both as a midgap gate material and as barrier layer against Cu diffusion. Al gate devices, with Al deposited by e-gun evaporation, were also fabricated.

The capacitors were then characterized using high frequency and quasistatic C-V measurements, for both p- and n-type Si substrates, from which the oxide and interface trap densities Q_f and D_{it} were extracted. The breakdown voltage V_{bd} was determined from I-V sweeps performed on n-type samples, with the gate voltage starting from 0 V and increasing at a rate of 0.1 V/sec. The cumulative percentage of devices failing at any gate voltage was extracted. An anneal at 510°C or at 650°C for 1 hour in N_2 was then performed to investigate both the possibility of copper penetration of the tungsten barrier in Cu/W devices and the behavior of W gate devices after thermal stress; the characterization was then repeated.

Results and Discussion: Figure 1 shows the breakdown voltage V_{bd} determined from I-V measurements for MOS diodes having Al, W or Cu/W gates. High quality W gate devices are obtained, with average breakdown field of 13 MV/cm. The Cu/W gate devices show significantly lower breakdown strength, indicating that the Cu deposition and patterning process increases the defectivity of the oxides; the Al gate devices also exhibit lower V_{bd}, though higher than that of Cu/W gate ones, due to defects and charging introduced by the e-gun evaporation. In figure 1 the effect of the annealing is also shown. W gate devices exhibit a slight V_{bd} increase after anneal at 510°C, with a larger decrease after anneal at 650°C. Cu/W devices do not show a V_{bd} change in the 510°C case, indicating that W acts satisfactorily against copper diffusion towards the gate dielectric at temperatures as high as 510°C; however, after heating at 650°C a decrease in average V_{bd}, accompanied by a wider V_{bd} distribution, is observed, indicating that the breakdown strength of the Cu/W gate devices is now compromised. While the cause is not evident, as this V_{bd} degradation is also observed in W gate devices, this may indicate that a copper penetration of the W barrier layer starts to occur with a prolonged anneal at 650°C.

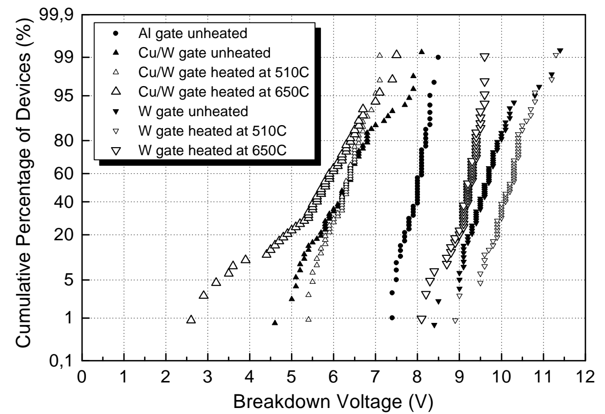

Figure 1: Cumulative V_{bd} statistical distributions for MOS diodes with W, Al or Cu/W gates, before and after anneal.

Figure 2 shows the C-V characteristics at 1 MHz of Cu/W gate devices before and after anneal. While no significant flatband voltage shift occurs in the 510°C case, a shift of –0.38 V appears after a 650°C anneal, indicating positive charge trapping in the oxide. This is probably associated with increase of defects due to Cu penetration and agrees with the compromised oxide integrity inferred from the V_{bd} data of figure 1 in the 650°C case. The high-low C-V method indicated a D_{it} at midgap in the low 10^{11} $eV^{-1}cm^{-2}$ range, reasonable since no forming gas anneal was performed, not significantly affected by the anneals.

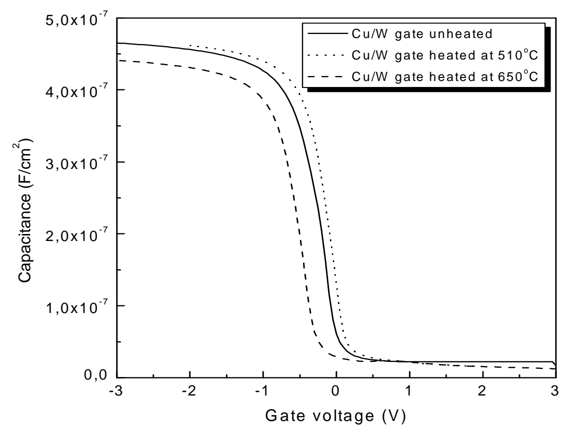

Figure 2: C-V characteristics for Cu/W gate capacitors.

Conclusions: The characteristics of midgap metal W or Cu/W gate MOS capacitors produced by a process using LPCVD of W and Cu liftoff were investigated. High quality W gate devices and effective W barrier action in Cu/W gate devices at 510°C were demonstrated.

References

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