## THERMODYNAMIC AND EXPERIMENTAL APPROACHES OF BARRIER MATERIALS SYNTHESIS FOR SILICON IC TECHNOLOGY

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As feature sizes continue to shrink (65 nm printed gate length is expected for 2007 (1)), intense research and development activities are focused on the introduction of new materials together with integration of new processes and structures in the different technology levels from Front End Processes (FEP) to Interconnect (usually referred to Back End Processes).

Implementation of copper/low  $\kappa$  dielectric using the damascene architecture has almost universally replaced traditional aluminum/SiO<sub>2</sub> structure. However, implementation of copper causes problems since copper diffuses easily in silicon and more generally in silicon oxides. It reacts with Si to form copper silicide Cu<sub>3</sub>Si at relatively low temperatures (<200°C). Successful incorporation of copper is conditioned to the insertion of a diffusion barrier between copper and surrounded layers (2). Except the naturally basic performance as diffusion barrier, this material should be deposited with excellent conformality in high aspect ratio damascene features.

There are three main requirements for an ideal diffusion barrier. First, the material should be conductive, with the lowest resistivity. Second, the material should not react with any of the other materials (Cu, Si, or dielectric) under BTS (Bias Thermal Stress) at temperatures around 500°C (last IC annealing steps). Finally, since grain boundary diffusion is typically rapid, an ideal barrier should have an amorphous microstructure. These requirements are typically in conflict with each other – finding such material that is conductive and amorphous and nonreactive is difficult

Proposition of guidelines for the material selection is given through a systematic thermodynamic study. Materials are classified in terms of interfacial stability and amorphization tendency.

Optimization of the already developed processes (e.g. TiN CVD) is presented .

- 1. ITRS, "International Technology Roadmap for Semiconductors," (2001)
- J. M. E. Harper, E. G. Colgan, C.-K. Hu, J. P. Hummel, L. P. Buchwalter, and C. E. Uzoh, *MRS Bulletin XIX* 23 (1994).