Trace-metal Defects within Silicon-on-Insulator Integrated Circuits

Paul E. Riley, Paul L. King, Boon-Yong Ang, and Jack Thomas

Advanced Micro Devices
915 Deguigne St.
Sunnyvale, CA 94088

The advantages in transistor scaling afforded by the use of silicon-on-insulator (SOI) wafers, namely improved transistor isolation and associated process simplifications, have been described by several authors previously.[1] In the development of advanced microprocessor circuits with SOI wafers, an unusual phenomenon was observed within the thin device layer of partially-processed SOI wafers for some lots. As shown by routine defect inspections by scan and SEM systems, small, crystallographically well-defined needles - ultimately found to contain nickel – were observed within the device-silicon layer, emanating from the silicon-insulating SiO_2 interface. The dimensions of these needles were ~ 50 – 200 nm x 100 nm in cross-section, similar to the dimensions of the features of the circuits being fabricated and in general parallel to the (100) silicon surface. The needles were often long enough to bridge adjacent transistors.

From AES, the material was shown to contain nickel, probably as nickel silicide, since processing temperatures at this juncture of fabrication were sufficiently high (~ 900 C) to form nickel silicide. These needles were clearly revealed after the plasma etch process used to form vertical isolation trenches within the silicon. Because the nickel-containing defects etched very slowly during the silicon trench etch process, these features remained largely in tact at the end of etching. The stability of these nickel-containing defects was confirmed with chemical analysis and electrical measurements from experiments carried out with contaminated and monitor wafers, processed together, at subsequent high temperature steps in the normal process sequence.

As shown by others,[2] Ni ions unlike other metal ions (e.g., those of Fe and Cu) do not diffuse through SiO_2 at normal processing temperatures to the back side of the silicon wafer which supports the SiO_2 and SOI layers, where metal gettering may occur. That is, diffusion of Ni ions is blocked by the SiO_2 barrier layer, such that under normal high temperature processing they may react to form nickel silicide at the SiO_2 interface and within the device Si layer.

The nickel contamination probably results from occasional metallic contamination of SOI wafers during normal wafer processing steps, originating from normal back side contact of wafers with shared pieces of processing, wafer-handling, and inspection equipment. This contamination probably adheres to the back sides of some wafers from which it may then be dispersed to the front sides of other SOI wafers. To ensure that, despite the stability mentioned above, nickel silicide contamination does not act as an additional source of metallic contamination across the fab, wafer inspection and processing protocols were developed to cope with this occasional form of heavy metal contamination.

References

1. See references in “CMOS Devices and Technology for VLSI,” John Y. Chen, Prentice Hall, Englewood Cliffs, NJ (1990).
2. J-I. Furihata, M. Nakano, and K. Mitani, ***Jpn. J. Appl. Phys***., **39**, 2251 (2000).