

High-Speed Conversion of Picosecond-Millivolt  
Pulse Signals to CMOS Voltage Levels

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Among the situations that require high-speed interfaces between superconductor circuits carrying millivolt single-flux-quantum (SFQ) pulses and volt-level semiconductor circuits are drivers for room-temperature or intermediate-temperature semiconductor circuits and interfaces between SFQ logic and a proposed hybrid Josephson-CMOS memory. The particular focus of this paper is on the latter application, in which case, the principal concern is the switching delay.

We are reporting developments on a previously proposed hybrid Josephson-CMOS interface amplifier and evaluating a possible alternate approach (1). The hybrid circuit employs a long series array of 400 Josephson tunnel junctions as a load on an NMOS driver. The array is formed on a silicon substrate in a hole in the ground plane. We will report calculations of the parasitic inductance and capacitance associated with the load array and their effects on the amplifier switching delay. The dominant cause of delay is the capacitance that must be charged to develop the output voltage; schemes for reduction of the capacitance will be reported. Also, a cryogenic CMOS amplifier circuit will be discussed for comparison with the hybrid amplifier. The purpose of this paper is to report the simulated relative delay performance of these designs and measurements of interface performance.

1. U. Ghoshal, H. Kroger, and T. Van Duzer, *IEEE Trans. Appl. Superconduct.*, **3**, 2315 (1993).