Abs. 45, 206th Meeting, © 2004 The Electrochemical Society, Inc.

SOI image sensor with pinned photodiode on handle wafer for high performance

Y. S. Cho and S. Y. Choi.

School of electronic and electrical engineering,
Kyungpook National University, Taegu, Korea

CMOS active pixel sensor (APS), fabricated using a standard CMOS process, have the advantage of low power consumption, low cost and a high level of integration. Due to intensive works over the past several years, The CMOS APS imagers are now considered as a visible alternative to charge-coupled device (CCD) in many application fields. Since they do not achieve the high quality image of CCD image sensors, however, they can be used only in applications that do not require high quality. They have difficulty in suppressing the dark current of the photodiode and fixed pattern noise (FPN).[1-2]

Silicon-on-insulator (SOI) technology has been proven to be advantageous in many applications. The sources of increased SOI performance are the elimination of area junction capacitance and that of body effect in bulk CMOS technology. As a result, image sensors that are built on SOI will find a useful application. A photodetector cell based on SOI technology provides a response corresponding to the incident light frequency. To integrate image sensors on SOI substrate, however, suffers from low quantum efficiency (QE). Due to the limited depth of silicon available on the top film, most of the photons can pass through the sensing regions without being absorbed.[3-4]

In this paper, we present a design and process optimization to improve both noise reduction and QE. A hybrid bulk/fully-depleted silicon-on-insulator (FD-SOI) complementary metal oxide semiconductor (CMOS) active pixel sensor has been fabricated. The active pixel comprises of reset and source follower transistors on the SOI seed wafer, while the pinned photodiode, readout gate, and floating diffusion (FD) are fabricated on the SOI handle wafer. The employing pinned photodiode as a photodiode is an easy and effective way of reducing the noise of dark current. The pinned photodiode on the SOI handle wafer can be optimized for quantum efficiency, because low handle wafer doping yields a large depletion width. The elimination of wells on the SOI seed wafer also allows for the use of pMOSFET without increasing the pixel size.

The pixel circuit outputs a pixel signal with a reset level and a signal level successively in one pixel period. A conventional four-transistor pixel has a readout gate, a reset transistor, an amplification transistor, and a row address transistor. Figure 1 shows the I_D-V_{DS} characteristics of a FD-SOI nMOSFET.

The photodiode is formed by an extra etching step with one extra mask to remove the buried oxide layer (BOX) on the SOI handle wafer. Readout gate and FD is also fabricated on the SOI handle wafer. The photodiode structure of p+/n-well/p-sub has a shallow junction with the depletion depth and the absorption depth. The depth is controlled by an implantation process and drive-in time. The channel stop of the p-implant around the pinned photodiode and FD eliminates the Si-SiO_2 interface related dark current generation. The pinned photodiode pattern layout is designed on $N_A=7\times10^{14}$ cm^{-3} of handle wafer. Figure 2 shows the photodiode operation by a readout gate voltage.

We measured the spectral response of a pinned photodiode and observed very flat in the wavelength range from green to red, because low substrate doping yields a large depletion width for a field-aided carrier collection from a deep region in the handle wafer. The monochromator illuminates the fabricated chip from 300 nm to 700 nm by 50 nm steps. Figure 3 shows the measured quantum efficiency normalized with a peak value.

References

[1] Kazuya Yonemoto and Hirofumi sumi, *IEEE J. Solid-State Circuits vol. 35, pp. 2038-2043* (2000)

[2] Yoshinori Iida, Eiji Oba, Keiji Mabuchi, Nobuo Nakamura, and Hiroki Miura, *IEEE J. Solid-State Circuits vol. 32, pp. 2042-2047* (1997).

[3] Chen Xu, Weiquan Zhang, and Mansun Chan, *IEEE Trans. Electron Device Letters, vol. 22, pp. 248-250* (2001).

[4] Xinyu Zheng, Suresh Seshadri, Michael Wood, Chris Wrigley, and Bedabrata Pain, *IEEE CCD AIS Workshop (Schloss-Elmau, May, 2003)*

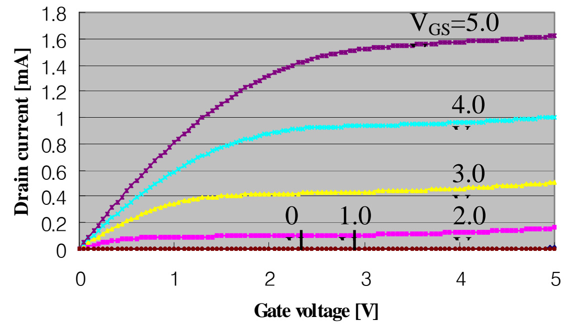

Fig. 1. I_D-V_{DS} characteristics of fabricated fully-depleted SOI nMOSFET. The channel length is 5 μm and the threshold voltage of the nMOSFET is 0.65 V

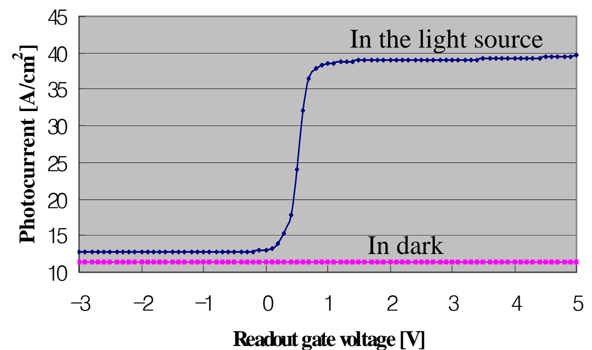

Fig. 2. Photocurrent versus a readout gate voltage with the reset transistor turned on at V_{DD}=2 V. The light source (630 nm = 290 μw/cm^2, 520 nm = 370 μw/cm^2, 450 = 450 μw/cm^2) is illuminated. The threshold voltage of the read out gate is 0.4 V.

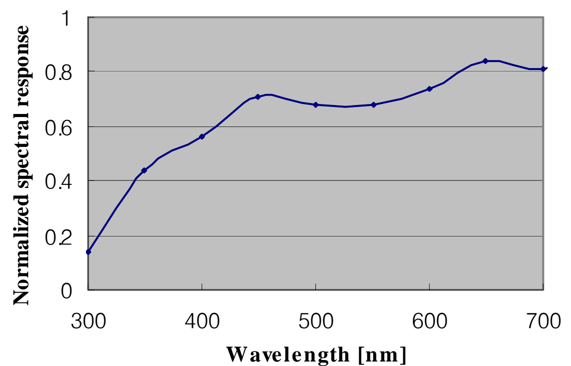

Fig. 3. Normalized quantum efficiency of a photodiode fabricated in the SOI handle wafer versus wavelength. The monochromator illuminates the fabricated chip from 300 nm to 700 nm by 50 nm steps.