Effects of NH_3 Pre-deposition Anneal on ALD High-k Gate Stacks

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The ITRS roadmap calls for implementation of high-k gate dielectric materials starting with the 65nm technology generation. This requires high quality interfaces between the high-k dielectric and Si substrate in the channel region. We have investigated the effect of various surface preparation treatments prior to high-k film deposition on transistor performance. Surface preparation treatments affect the growth of the high-k film and the final EOT.

This work discusses the effect of NH_3 anneals and process conditions on high-k transistor performance such as gate leakage, Vt and electron mobility [1]. Transistors were fabricated on 200 mm p-type epi <100> Si substrate using a conventional silicon gate transistor process flow with thin high-k dielectrics deposited by the atomic layer deposition (ALD). The ALD-HfO_2 film exhibits an incubation period and island type growth on HF-last surfaces [2], and the resulting films exhibit high gate leakage current or non-working devices. The addition of an NH_3 pretreatment is shown to affect the properties of the interfacial layer at the silicon/high-k interface, which is critical for controlling the final EOT. An NH_3 anneal pretreatment, i.e., an NH_3 predeposition anneal (PreDA), after an HF-last clean led to ~5Å bottom interfacial layer after high-k deposition which is about 50% thinner than what was observed with the ALD films grown on the chemical oxides interfaces, without the NH_3 PreDA. Lower EOT and lower leakage current also are obtained when an NH_3 PreDA follows the HF-last for ALD HfO_2 films. These surface preparation processes result in an EOT reduction of 4Å to 5Å versus chemical oxides, providing a potential solution to achieving a sub-1nm EOT. NH_3 anneal temperatures ranging from 500ºC to 900ºC have been studied to correlate the effect of N concentration in the bottom interface on the transistor properties.

Figure 1 shows the nitrogen concentration obtained by SIMS analysis. The nitrogen concentration increase in a steady manner between 600ºC and 900ºC, while a rapid increase is observed between 500ºC and 600ºC. Figure 2 shows the drive current density versus EOT for different transistors fabricated using different NH_3 temperature anneal and a series of ALD- HfO_2 film thickness (20Å, 25Å and 30Å. The data show an increase in drive current by using lower NH_3 anneal temperatures or lower N concentration at the silicon/high-k interface.

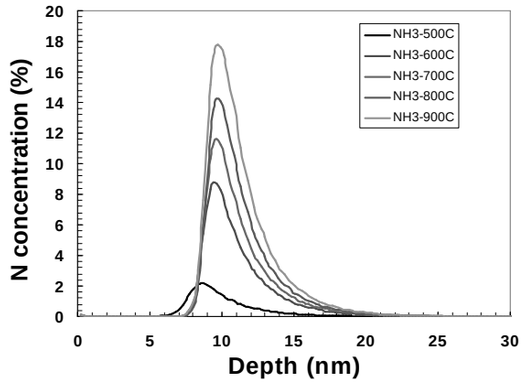

Figure 1: SIMS nitrogen concentration profile after NH_3 anneal at different temperatures

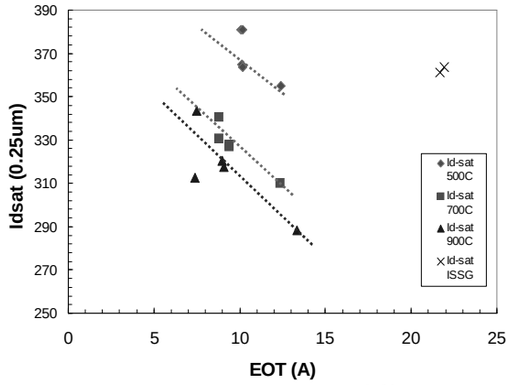

Figure 2: Drive current versus different NH_3 pre deposition anneal conditions obtained for the 30Å, 25Å, and 20Å ALD-HfO_2 with TiN electrode stack deposited on the HF-last/NH3 interface

REFERENCES

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