The Fabrication of Nanometer Silicon Pillar Channel for Buried Gate Type Surrounding Gate Transistor by Silicon Isotropic Etching

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Abstract

This paper shows the fabrication process and the result of experiment of the pillar formation of Buried Gate type SGT[1] which was proposed to realize ultra high density LSI.

Introduction

Surrounding Gate Transistor (SGT)[2] have received much attention as future devices for the various applications like Stacked-SGT (S-SGT) DRAM[3], S-SGT type flash memory [4] and so on. The SGT arranges source, gate and drain vertically. Therefore, the occupied area of SGT can be smaller than that of planar MOSFET. Fig.1 shows the schematic cross-sectional view and top view of the conventional SGT(a) and the Buried Gate type SGT(b). The silicon pillars are composed of drain, body and source from the upper part. Gate oxide and gate electrode surround the silicon pillar as shown in Fig.1(a)(b).

In the case of Buried Gate type SGT as shown in Fig.1(b), the diameter of the body region is smaller than that of drain region, that is, minimum feature size F (we call this region "buried region".)

By the fabrication of the buried region which has a smaller diameter than the minimum feature size F, body region becomes fully depleted condition. Therefore the Buried Gate type SGT can realize the ideal subthreshold slope[1].

Fabrication Process

Fig.2 shows the fabrication process of formation of the buried region. The structure was fabricated on (100) p-type silicon substrate. After mask formation through thermal oxidation and etching silicon oxide by Reactive Ion Etching (RIE) , the silicon pillar which will be later on become drain was formed by RIE (Fig.2(a)). Non-doped Silicon Glass (NSG) were deposited conformally by Low-Pressure Chemical Vapor Deposition (Fig.2(b)) followed by RIE (Fig2.(c)) to form sidewall mask of NSG around silicon pillar. Then by isotropic etching of silicon , the substrate was etched to form (Fig.2(d)).

Result

Fig.3 shows the SEM picture of the buried region experimentally fabricated by the fabrication process described above. Silicon dioxide was removed by wet etching. As seen from Fig.3, the buried region which has a diameter of 17nm was formed successfully, while the diameter of the upper part of the silicon pillar was 65nm.

Conclusion

In this paper, we have reported on the fabrication process of the Buried Gate type SGT and the result of the experiments. This process is useful to fabricate the buried region.

Acknowledgements

We carry out this fabrication process in super clean room of Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University.

Reference

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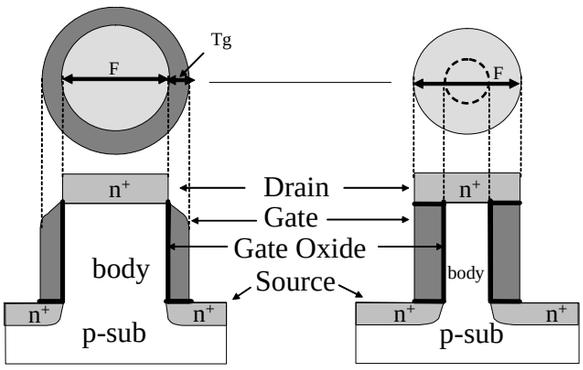

(a) (b)

Fig.1: The schematic top view and cross-sectional view of the structures of (a)conventional SGT and (b)Buried Gate type SGT

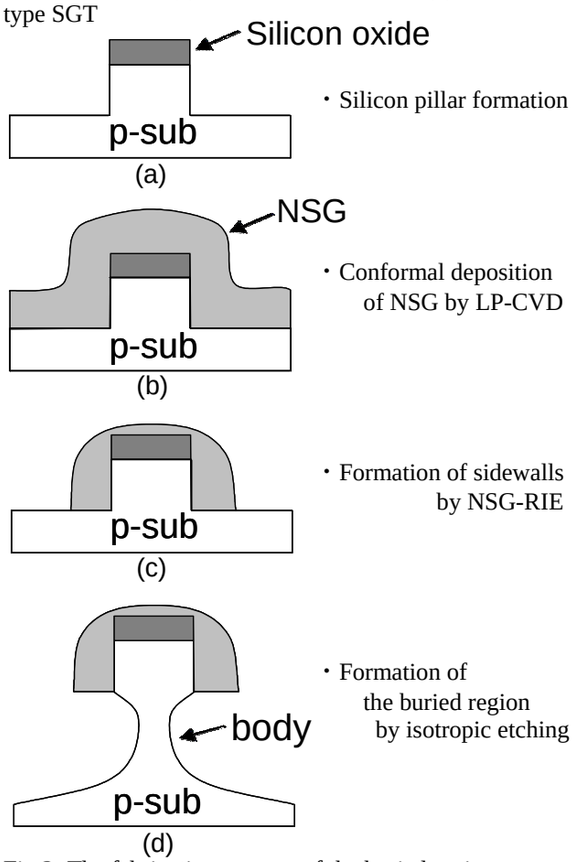

Fig.2: The fabrication process of the buried region.

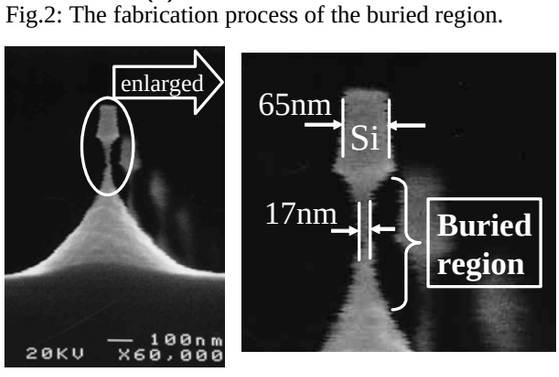

Fig.3: SEM photograph of the silicon pillar with the buried region . The diameter of the buried region is 17nm and that of the upper part remained as it was is 65nm .