# Investigation into the Electrical and Thermal Properties of Strained Si pMOSFETs

G. Nicholas, T. J. Grasby, E.H.C. Parker and T.E. Whall
Nano-Si Group, University of Warwick
Coventry, West Mids, CV4 7AL, U.K.

The difficulties associated with the continued downscaling of conventional Si MOSFETs has led to other materials being seriously considered as an alternative means of improving device performance. Of these alternatives, strained Si, created either by growth of a thin layer on a SiGe virtual substrate or by mechanically induced strain, appears to be amongst the most promising.

There has been much work published on nMOSFETs with a biaxial tensile strained Si channel.[1] For electrons, the mobility enhancement saturates when the terminating germanium composition of the virtual substrate reaches 20%. However, unlocking the largest hole mobility enhancements in tensile strained Si requires terminating compositions of up to 45%. For this reason, there has only been limited investigation of strained Si pMOSFETs.

If strained Si devices on virtual substrates are ever to enter production, it is important to know the properties of the Si/SiGe band system. The valence and conduction band discontinuities between strained Si and relaxed SiGe play an important role in determining the threshold voltage of a device. So far there has been no definitive treatment of these parameters, with the majority of work being theoretical and only one experimental determination of the conduction band offset for $Si/Si_{0.67}Ge_{0.33}$.[2]

The band alignment between strained Si and relaxed SiGe is type II, such that it is sometimes energetically favourable for holes to occupy the lower mobility alloy. This is not likely to be a problem in an aggressively scaled device, with a thin gate oxide and large vertical effective field, because the band-bending at the surface is sufficient that the majority of holes will be confined to the strained Si layer. However, to investigate the magnitude of the valence band offset, long channel strained Si pMOSFETs are fabricated on $Si_{1-x}Ge_x$ virtual substrates ($0.18 \leq x \leq 0.36$) with thick gate oxides. The heavy parasitic conduction results in the formation of two distinct peaks in the transconductance characteristic, corresponding to occupation of the two layers. Comparison of the measured transconductance with that simulated by a two-dimensional drift-diffusion device simulator enables extraction of the valence band discontinuity (fig. 1.). This is found to be larger than previous theoretical predictions.[3]

A problem that must be overcome before strained Si on a virtual substrate may be used in production is the issue of self-heating. The thermal conductivity of SiGe varies somewhat with composition but it is, in general, at least fifteen times lower than that of Si. This effectively thermally insulates the strained Si from the substrate, resulting in power dissipated by the MOSFET heating the channel. The increase in phonon scattering reduces the carrier mobility and leads to a reduction in drain current. This problem is known to be worse for strained Si nMOSFETs due to their higher power dissipation but may also effect pMOSFETs.

To overcome the issue of self-heating will require thin virtual substrates or alternative methods of cooling. Using the model devised by Su *et al.* [4] to estimate the thermal resistance of a strained Si MOSFET, a consideration of the necessary reduction in virtual substrate thickness to keep the local temperature rise to acceptable levels is given.

A popular method for the measurement of SOI and strained Si MOSFETs in the absence of self-heating is the pulsed measurement technique, by which very short (~ 10 ns) bias pulses are applied to the device and the resultant drain current measured before significant heating occurs. Using a pulsed measurement system, the first published result showing significant self-heating in a strained Si pMOSFET is presented (fig. 2). By heating strained Si MOSFETs whilst performing pulsed measurements, the thermal resistance is extracted and compared to that predicted by the model. The measured thermal resistance is found to be lower than expected due to the proximity of an additional well contact, indicating the feasibility of reducing self-heating by innovative design.

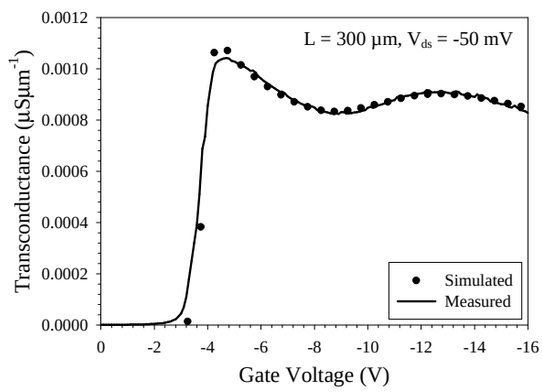


Fig. 1. Comparison of measured and simulated transconductance for a strained Si pMOSFET (x = 0.36).

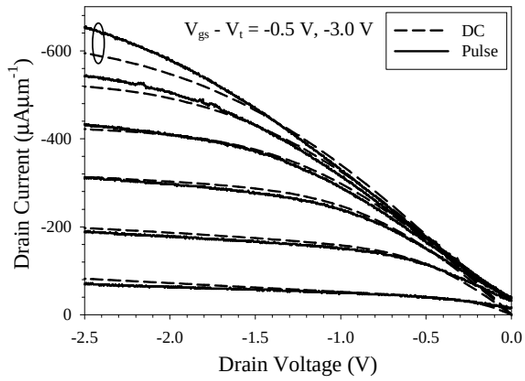


Fig. 2. Pulsed measurement of a 0.175 × 10 µm strained Si pMOSFET, showing significant self-heating.

1. K. Rim *et al.*, *Solid-State Electronics*, **47**, 1133 (2003).
2. L. Garchery, I. Sagnes and P. A. Badoz, *Applied Surface Science*, **102**, 202 (1996).
3. M.M. Rieger and P. Vogl, *Phys. Rev. B*, **48**, 14276 (1993).
4. L. Su *et al.*, *IEEE Trans. Elec. Dev.*, **41**, 69 (1994).