Dual High-k Gate Oxide Characteristics of Al_2O_3 films on Si (100) Substrate

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Recently, high-k gate dielectrics have been studied as a gate insulator due to its higher dielectric constant, thermodynamic compatibility of the interface with Si, and a relatively large band gap.[1, 2] Many studies have been devoted to the electrical characterization and the understanding of transistors with a dual gate SiO_2 oxide in logic devices such as a system-on-a-chip. However, it is little known about the wet etching effect and interface variation on the electrical characteristics of the dual high-k gate oxide. In this study, the electrical characteristics of the MOS capacitors with the dual thickness of Al_2O_3 gate dielectric films, Pt gate/ single deposited thin Al_2O_3/p-type Si (s1), Pt gate/ dual deposited thin Al_2O_3/p-type Si (d1), Pt gate/ single deposited thick Al_2O_3/p-type Si (s1k), and Pt gate/ dual deposited thick Al_2O_3/p-type Si (d1k), where the Al_2O_3 were grown by atomic layer deposition (ALD), were examined. Al_2O_3 films were deposited on p-type Si (100) wafers with a resistivity of 4~8 Ω cm by an ALD technique using a traveling-wave type ALD reactor after RCA standard cleaning. $Al(CH_3)_3$ and H_2O were used, as the precursors and oxidant for the Al_2O_3 films at a wafer temperature of 400°C. The physical thickness of the thin and thick Al_2O_3 samples was approximately 4.5 ~ 4.7 nm and 7.7 ~ 8.3 nm, respectively, in the single Al_2O_3 films. In the dual Al_2O_3 process, the first and second Al_2O_3 thickness of the thin and thick Al_2O_3 samples was controlled to be similar above thickness. Post deposition annealing (PDA) of the samples was performed with rapid thermal annealing (RTA) at 700 ~ 900°C in N_2 for 30 sec, where, in order to get rid of O_2 in the PDA process, firstly, the air of chamber was exhausted with turbo-vacuum pump by 10^{-5} Torr, secondly, the PDA was proceeded under 10^{-1} Torr with dry vacuum pump injecting N_2 gas. The HF dilute solution (D.I water: HF = 50:1, 100:1, 200:1 at 25°C) was used to etch the first Al_2O_3 film in the dual high-k gate oxide process. Pt gate (~ 100 nm) was fabricated using evaporator after PDA. Post-metallization annealing was performed at 400°C in H_2 for 30 min. Figure 1 shows the average film thickness changes of samples (4.5 ~ 4.7 nm) with the variable diluted HF concentration and PDA temperatures as a function of the wet etch time. The estimated etch rates of each sample from the decreased thickness for 5 seconds are; 100:1 HF – as-deposited: 0.60 nm/sec, 100:1 HF – 700°C PDA: 0.44 nm/sec, 100:1 HF – 800°C PDA: 0.43 nm/sec, 100:1 HF – 900°C PDA: 0.21 nm/sec, 50:1 HF – 800°C PDA: 0.50 nm/sec, and 200:1 HF – 800°C PDA: 0.10 nm/sec. It was investigated that the etch rates affected by the variable diluted HF concentration after and the annealing conditions with or without PDA. It was necessary the minimum 20 seconds in the 100:1 HF to etch thin Al_2O_3 films and finally decided to 30 sec for reproducible MOS capacitor. The surface roughness of Si substrate measured by AFM after the diluted HF etching were approximately 1.8, 1.9, and 2.4 Å, respectively, for the 200:1, 100:1, and 50:1 HF solution for 30 sec. The surface roughness can much affect the interface characteristics and electrical reliability between Al_2O_3 layer and Si substrate. Figure 2 shows the C-V plots measured at 1MHz and the leakage current densities (J) of MOS capacitors. The thin and thick Al_2O_3 film of dual high-k MOS capacitors showed the good electrical properties, a leakage current density of -3.3×10^{-6}A/cm^2 and -2.5×10^{-9}A/cm^2 at –1 V, respectively due to a lower hysteresis voltage and the interface state density. It is suggested that the dual Al_2O_3 films be applicable to the gate oxide of the low power MOS device.

1. G. D. Wilk *et al.*, Appl. Phys. Lett., 74, 2854, 1999
2. M. Cho *et al.*, Appl. Phys. Lett., 81, 334, 2002

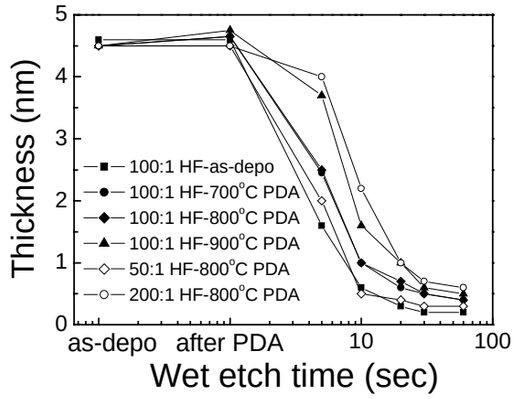

Fig. 1. The gate oxide thickness distribution of Al_2O_3 films with the diluted HF concentration. The etch rate increased with a higher HF concentration and lower PDA temperature.

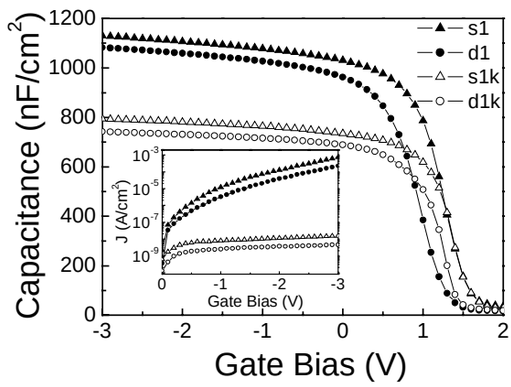

Fig. 2. The capacitance and leakage current density of MOS capacitors as a function of the gate bias.