ADVANCED PROCESS MODULES FOR SCALED ULSIs

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INTRODUCTION

For sub-100nm scaled-ULSIs, new processes and materials are important to create high-performance and low-power CMOS devices. There are several critical issues for sub-100nm CMOS devices. For FEOL, main issues are channel design and the advanced gate-stack structures. Controlled channel impurity profiles and High-k gate insulators as the new material are required. For BEOL, those are the interlayer insulators with low-k value. In this paper, these issues will be discussed.

SUB-10nm MOSFET DEVICE DESIGN

Device scaling is needed to increase device performance. Sub-25nm gate length CMOS devices have been presented for high- performance ULSIs[1,2]. Precise impurity profile control is required to realize sub-10nm MOSFETs.

Sub-10-nm planar-bulk CMOS devices are fabricated by using a S/D-junction control technique, such as notch-gate structure and reverse-order SD formation. Notch-gate structure has the advantage of the individual profile formation for SDE and halo. The gate length is highly-controlled even having the notch. The notch gate electrode (Fig.1) significantly suppresses the short-channel effects and variation of off currents, simultaneously. The low temperature spike annealing also drastically suppresses the short-channel effects for both n-and p-MOSFETs. Figure 2 shows the drain current characteristics at 0.4 V for n- and p-MOSFETs. Good cut-off characteristics are obtained for 5nm n- and p-MOSFETs. The 5nm bulk CMOS device has a smaller off current, compared with the previously reported sub-10-nm devices. To enhance the drive current in advance devices, the SDE resistance should be reduced by using the new techniques.

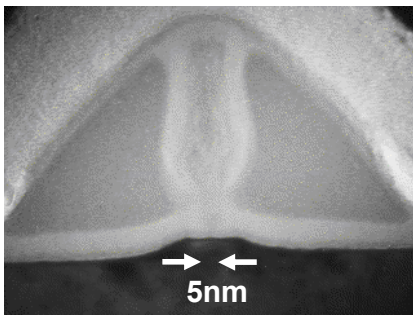

Fig.1: Cross sectional TEM image for 5nm gate electrode with notch.

NEW TECHNOLOGIES for FEOL & BEOL

High-k gate-stacked devices and Low-k/Cu interconnects are described from the viewpoint of process modules of scaled ULSIs [3,4]. For High-k gate-stacked MOSFETs, poly-Si gated MOSFETs with HfSiO(1.8nm) insulator were demonstrated. A symmetrical set of Vth's for NFET and PFET was realized for low power device operation. Poly-Si/HfSiO gate-stacked CMOS devices have shown low Ioff(N/PFET: 4.8/3.6pA/μm) and high Ion(N/PFET: 469/140 μA/μm). For advanced Low-k interconnect technology, a highly reliable Low-k/Cu interconnect were shown with 180nm/200nm- pitched lines connected through φ100nm-vias. A porous SiOCH film (k=2.5) with sub-nanometer pores is introduced for the inter-metal dielectrics (IMD).

SUMMARY

Process modules of scaled ULSIs, including ultra-small MOSFET device design, High-k gate-stacked devices and Low-k/Cu interconnects were discussed. 5nm planar bulk-CMOS devices, poly-Si/HfSiO gate- stacked CMOS devices and the highly reliable porous-Low-k/Cu interconnect were demonstrated. For scaled ULSIs, new processes and materials should be introduced to create higher-performance and lower-power CMOS devices.

REFERENCES

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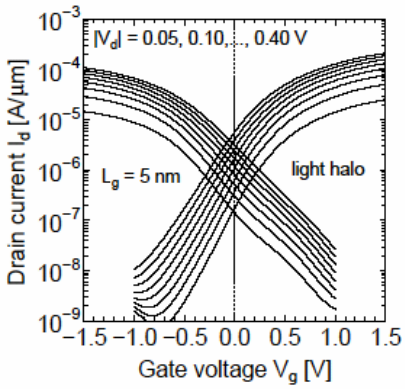

Fig.2: Subthreshold characteristics for n-/p-MOSFETs with 5nm gate length.