Double-Gate FinFET Innovation: From 3-Terminal to Flexible Threshold Voltage 4-Terminal

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The high-performance of double-gate FinFETs has already been confirmed both by theoretically and experimentally [1-4]. However, the double gates of the conventional FinFETs are connected together, i.e., the FinFETs are operated as a 3-terminal device. Thus, the threshold voltage (V_{th}) in the FinFETs can not be controlled by gate biasing. To overcome this drawback, the 4-terminal FinFETs with independent double gates have been developed [5-7]. In this paper, the research and development of our FinFETs technology including 4T-FinFETs are reviewed.

The fabrication processes are as follows. The starting material was the p-type (110) SOI wafer. First, the wafers were thermally oxidized and fin patterns were formed in parallel with <112> direction by EB-lithography and RIE. Then, the SOI was etched with a 2.38% TMAH solution to form upright Si-fins. Since the sidewall of the Si-fin is the (111) plane with an extremely low etch rate, very narrow and straight Si-fins can be fabricated. After the gate oxide formation, the n^+ poly-Si gate was made by EB-lithography and RIE. The n^+ doping for source-drain extension regions was performed by rapid thermal annealing (RTA), and finally aluminum electrodes were formed and sintered in a pure H_2 ambient at 400 C.

Figure 1 shows the cross-sectional STEM image of the fabricated FinFET with 13-nm thick Si-fin channel. It is clear that the Si-fin shows the ideal rectangular channel shape. The measured I_d-V_d characteristic of the 13-nm thick Si-fin channel FinFET is shown in Figs. 2. The measured on-current (I_{on}) normalized by $2H_{fin}$ (H_{fin} is fin height) is as high as 720 μA/μm at $V_g = V_d = 1$ V, which might be attributed to crystallographic flatness of sidewalls causing less surface roughness scattering.

Figure 3 shows the cross-sectional STEM image of the fabricated 4T-FinFETs with independent double gates. In the gate separation, precise CMP process was used. We define the left gate (G_1) as driving gate and the right gate (G_2) as a control gate. The measured I_d-V_{g1} characteristics as a function of V_{g2} are shown in Fig. 4. It is noteworthy that the subthreshold curve shifts linearly with V_{g2} biases, which implies that the V_{th} can be controlled flexibly by changing gate biasing.

In summary, we have been succeeded in fabricating the FinFETs including V_{th} controllable 4T-FinFETs by using newly developed orientation-dependent wet etching. The high drive current and flexible V_{th} controllability have experimentally been confirmed. The 4T-FinFETs are promising for future high-performance and flexible power managing ULSI circuits.

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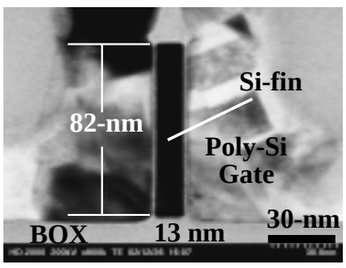

Fig. 1. Cross-sectional STEM image of the fabricated FinFET with an ideal rectangular channel shape.

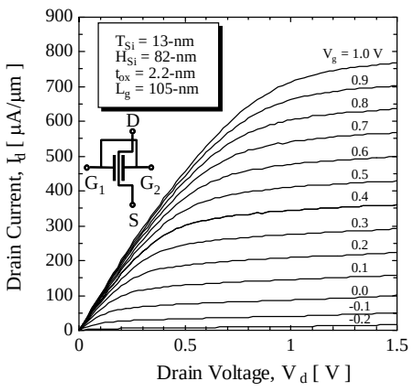

Fig. 2. I_d-V_g characteristics of the fabricated FinFET with 13-nm Si-fin thickness and 105 nm gate length.

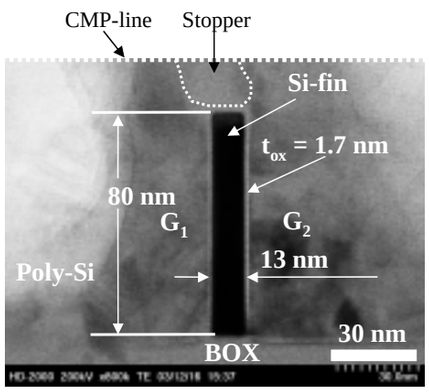

Fig. 3. Cross-sectional STEM image of the fabricated 4T-FinFET with a 13-nm thick Si-fin channel.

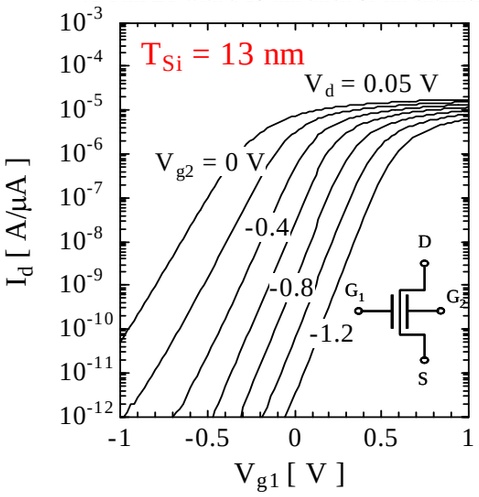

Fig. 4. I_d-V_{g1} characteristics as a function of V_{g2} for the 4T-FinFET with 13-nm thick Si-fin channel.