Plasma Activated Wafer Bonding for Thin Silicon-On-Insulator Substrate Fabrication

Paul Lindner, Dr.Shari Farrens[β], Dr.Viorel Dragoi

EV Group, DI Erich Thallner Strasse 1, A-4780 Scharding, Austria
[β]EV Group Inc. 3701 University Drive, Suite 300, Phoenix, AZ 85034, USA

Most of the microelectronic devices use only a thin silicon layer near the surface of a semiconductor wafer (in the range of hundreds of nanometers), the remaining thickness being used only as a mechanical support. Electrical interaction between the device layer and the thick substrate leads to parasitic effects. The thick conductive substrate also complicates the electrical insulation of independent neighboring devices.

An alternative solution to such problems is the use of a sandwich-like structure, the so called Silicon-on-Insulator (SOI). SOI substrates consist in a thin Si device layer electrically insulated from the thick Si substrate by an oxide layer. It has been demonstrated that the use of SOI substrates enables the fabrication of high performance, very high density circuits (DRAM's, microprocessors, etc.)

At the beginning of 90's, researchers at LETI Grenoble (France) proposed a new method for SOI fabrication, based on ion implantation and wafer bonding [1]: a Si wafer is implanted with hydrogen ions with doses in the range 3.5 x 10^{16} – 1 x 10^{17} cm^{-2}, and then it is bonded to a thermally oxidized Si wafer. Further thermal annealing will lead to the splitting of a thin Si layer from the implanted wafer and the result will be an SOI structure. The technique is known as Smart-Cut® and the commercial name of the SOI fabrication process is UNIBOND® (SOITEC, France). The main advantages of this method are: good thickness control of the top layer by controlling the implantation parameters and the reuse of the implanted wafer for further SOI wafer production.

Fully automated wafer bonding systems perform multiple critical tasks: Wafer cleaning prior to bonding is performed in cleaning stations combining brush scrubbing, megasonic cleaning and wet chemical cleaning procedures. Subsequent mechanical notch alignment, pre-bonding and automatic IR inspection of the bonded wafers contribute to a typical throughput of 25-35 bonded pairs per hour in three shifts production activities.

Since SOI reached its technological maturity, the new challenges for this field are raised by the technological shift to larger area (300mm) wafers and new materials combinations such as GeOI (Germanium-On-Insulator).

For 300mm SOI wafers increased bond strength at low temperature (<400C°) has the potential to improve SOI bonding yield and minimize the SOI wafer exclusion zone. The mismatched thermal expansion of dissimilar materials cause stress during annealing. Therefore higher bond strength at lower annealing temperature is desired.

Plasma activation prior to bonding is the most promising technique demonstrating an increase of bond strength kinetics.

The most common uses of plasma in CMOS and MEMS fabrication are for reactive ion etching, thin film deposition, and cleaning. This year will see the first commercial application of plasmas for wafer bonding.

Plasma activated wafer bonding has been in development since the late 1980's and offers several advantages over traditional bonding methods such as anodic bonding or high temperature silicon direct fusion bonding. The main advantage is the ability to create bonded substrates at temperatures below 400C that have achieved the full mechanical strength allowed by the system and with excellent electrical or optical properties. Many believe this technique will lead to a transition from silicon based electronics to hybrid materials such as GeOI, sSOI, and GaAs-Si. Certainly, the technique will provide device designers with increased choices for starting substrates, engineered materials properties and integration options.

Plasma activated wafer bonding is an application where the ionized gas atoms are used to modify the surface conditions of a substrate. In wafer bonding applications the goal is to create conditions that promote the development of chemical bonds between two surfaces. This is accomplished by providing reactive species that will not only participate in the chemical reactions ongoing at the bond interface, but also catalyze the reaction or speed up the kinetics of the bond development. Hence, plasma bonding is most often accomplished by using oxygen plasmas for applications that require electrical isolation at the interface, and hydrogen, nitrogen or argon plasmas in applications seeking a direct or conductive bond interface. In order to satisfy the requirements of a large segment of the semiconductor industry, plasma activated bonding equipment must have a large process window, integrate to additional process modules such as alignment stages, and conform to industry standards for safety and cleanliness.

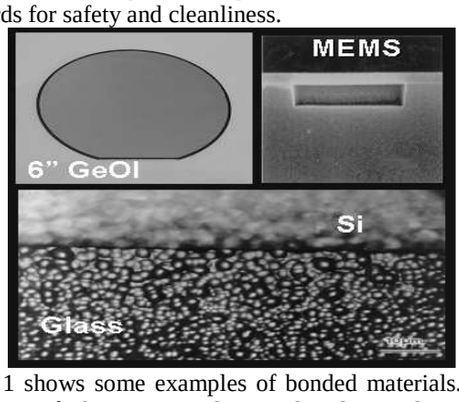

Figure 1 shows some examples of bonded materials. The interfaces of these materials can be designed to meet application specific requirements of conductivity, transparency and defect density regardless of CTE difference.

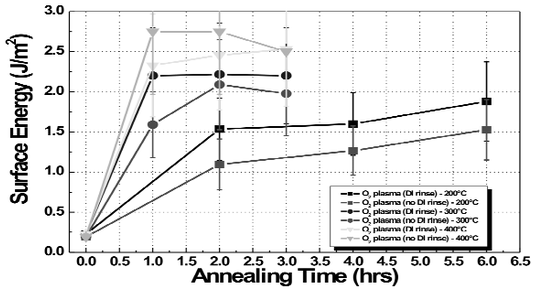

Figure 2 is a typical example of bond kinetics for silicon bonded to 400 nm of silicon dioxide. Each data point represents several measurements from 5 individual bonded pairs. The test procedure is the industry accepted method of Maszara, known also as crack opening method or blade method [2].

REFERENCE

1. M. Bruel, Electron. Lett. 31 (1995) 1201.
2. W.P. Maszara, G. Goetz,A. Cavilia, and J.B. McKitterick, J.Appl. Phys., **64**, 4943 (1988).