PROGRESS AND ISSUES IN DIELECTRIC MATERIALS FOR SUB-100NM DRAM TECHNOLOGY

Kanta Saino

Device Integration Group, Technology & Development Office, Elpida Memory Inc.

7-10 Yoshikawakogyodanchi, Higashihiroshima, Hiroshima, 739-0198, Japan

ABSTRACT

In this paper, critical issues and recent advances in dielectric materials such as capacitor, gate and interlayer dielectric (ILD) for sub-100nm Dynamic Random Access Memory (DRAM) are discussed. In the case of capacitor, technologies to increase surface area of capacitor will not offer enough storage capacitance Cs and it must be incorporated with Equivalent Oxide Thickness (EOT) decrease. Recently developed MIS Ta_2O_5 or Al_2O_3 capacitor will not match the required EOT for sub-100nm DRAM and it is expected to be replaced by Metal-Insulator-Metal (MIM) capacitor with high-k dielectric films in 70nm technology node. In the case of gate dielectric, simply scaling the gate oxide thickness will not satisfy the device requirements, and introduction of gate SiON would be indispensable. In the case of ILD, void-free gap filling becomes a critical issue because of high-aspect ratio gap in STI, inter-wordline and inter-bitline. Introduction of Spin-On-Glass (SOG) will help to ease this problem. Adopting new material affects yield and reliability of products therefore careful evaluation is necessary.

I. INTRODUCTION

In DRAM products, dielectric materials are used for many purposes, such as device isolation, gate dielectric, capacitor dielectric and interlayer dielectric. SiO_2 has been widely used for above all purposes in early stage of DRAM mass production. Beyond 100nm generation, DRAM technology continuously faces severe scaling problems, such as difficulties in obtaining sufficient Cs and transistor performance, and achieving device isolation. To overcome these problems, new dielectric materials must be developed. Here, requirements, issues and possible solutions for sub-100nm DRAM application are discussed in terms of capacitor, gate and interlayer dielectric.

II. CAPACITOR DIELECTRIC MATERIALS

One of the major challenges in manufacturing sub-100nm DRAM is to obtain sufficient data retention characteristics. Data retention time is determined by the voltage difference ΔV that appears on two bitlines, D and /D, and it is given by the following equation,

$$\Delta V = Cs/(Cs+Cb)\times 0.5Vd,$$

where Vd is the array operation voltage, Cs is the storage capacitance, Cb is the bitline capacitance. According to the above equation, larger Cs and smaller Cb are preferred to improve data retention characteristics. Therefore, many efforts to increase Cs in limited cell area have been done since the birth of DRAM. Cs is given by,

$$Cs = \varepsilon_0 \varepsilon_s \times S/d,$$

where S is the area of storage capacitor, d is the thickness of capacitor dielectric, ε_0 is the permittivity in vacuum and ε_s is the dielectric constant. To increase Cs, it is effective to increase surface area and to employ thin high-k dielectric. Therefore, there are two approaches in increasing Cs, one is increasing surface area and the other is exploiting new dielectric materials.

2.1 Evolution of storage capacitor structure and dielectric material

Figure 1 shows the evolution of DRAM cell structure and capacitor dielectric. To improve Cs, efforts have been focused on increasing surface area in the early stage of development. Planar-type capacitor, which has been used in early DRAM products, was replaced by two types of three-dimensional capacitors, stack-type and trench-type capacitors, in 1μm-rule generation. As scaling continues, stack-type capacitor evolved into Capacitor-Over-Bitlne (COB) structure. Recently, even cylinder-type structure is adopted and used in mass production. During that evolution, Hemi-Spherical-Grain (HSG) technology was employed to further increase the surface area of storage capacitors [1]. For capacitor dielectric material, films with low-leakage and high reliability, such as SiO_2, Oxide-Nitride-Oxide (ONO) and Nitride-Oxide (NO), have been used. As design rule is scaled down below 150nm, however, it became quite difficult to obtain sufficient Cs even with above-mentioned 3D cell structures. Therefore, high-k materials, such as Metal-Insulator-Semiconductor (MIS) Ta_2O_5 [2] and Al_2O_3 [3], were introduced.

For trench-type cell, capacitor dielectric film must be thermally stable up to 1000°C since capacitor is formed before source–drain activation. From such reason, ONO dielectric is also widely used as capacitor dielectric in trench-type cell. To obtain sufficient Cs, trenches became deeper every generation. In recent reports, bottle-shaped trench [4] and even HSG is adopted [5]. However, regardless of cell structure, technologies to increase surface area of capacitors are approaching its limit.

2.2 Requirements for sub-100nm DRAM capacitor dielectric

Although many changes in capacitor structure and material have been adopted during the course of device scaling, required storage capacitance to obtain decent data retention characteristics was nearly constant at 30fF/cell. It is estimated to be necessary to keep that trend constant regardless of design rule. Figure 2 summarizes the required EOT for different capacitor structure to acquire 30fF/cell in sub-100nm DRAMs. It seems

difficult to extend MIS Ta_2O_5 dielectric (EOT=3.5nm), which is currently used in mass production, into 70nm generation, because the height of bottom electrode must exceed 4.6μm and 3.6μm for Concave + HSG and Cylinder capacitor, respectively. Moreover, decreasing EOT of MIS Ta_2O_5 seems challenging since the existence of low-k SiON layer at the Ta_2O_5/poly-Si interface is inevitable to suppress leakage current. It is evident that search for the next dielectric film is therefore necessary. Assuming bottom electrode height to be 1.8μm, target EOTs for 70nm generation would be 1.25nm and 1.75nm for Concave + HSG and Cylinder structure, respectively. In order to decrease EOT, oxide layer at the dielectric/electrode interface must be avoided. Therefore, Metal-Insulator-Metal (MIM) structure, which utilizes metal for both upper and bottom electrode, is regarded as a promising candidate for sub-100nm DRAM capacitor technology. Both MIS and MIM capacitor must satisfy not only target EOT but also other requirements to be integrated in DRAM processes. Requests for capacitor dielectric material in sub-100nm generation are summarized in Fig. 3. High-k and high quality film with excellent controllability and productivity is inevitable. Since electrode height of 1.8μm is necessary even with MIM capacitor, dielectric and electrode films must have excellent step coverage. Also dielectric film must be thermally stable to CVD and metallization processes since deep metal contact becomes inevitable. Simple chemical structure is preferred for capacitor dielectric since it gives better controllability of stoichiometry and wider process window. Thickness of bottom electrode becomes also important because it determines the surface area of capacitor. Therefore, thin but mechanically robust electrode is requested.

2.3 Recent advances and issues in capacitor dielectric materials

Recent reports on high-k capacitor films are summarized in Table. 1. Various kinds of capacitor dielectric have been investigated for stack-type cell, according to its wider process temperature margin compared to trench-type cell. In the '90s, research interests were focused on high-k (ε_s>100) dielectric films such as (Ba,Sr)TiO_3 (BST) [6, 7] and $SrTiO_3$ (STO) [8, 9]. MIM structure having Ru-based metal (or Pt) as its top and bottom electrodes has been widely reported. However, those films had several integration problems such as barrier metal formation, controllability of film stoichiometry in 3D-structure cell, thermal stability, and immunity against forming gas annealing. Meanwhile, HfO_2 and its stack films, which have been intensively investigated as the next generation gate dielectric film for logic devices, are gathering the recent interests of many DRAM researchers. MIS Al_2O_3-HfO_2 (AHO) combines the advantage of wide band gap given by Al_2O_3 and high-k given by HfO_2 therefore gives low leakage property with relatively thin EOT [10]. Simple chemical structure offers excellent controllability. Atomic Layer Deposition (ALD) is generally used for deposition technique. In the recent report, EOT of 2.25nm with reasonable leakage of 1fA/cell (@1.65V) has been obtained. These characteristics are equivalent to Cs = 31fF/cell in 90nm-DRAM cell with 1.8μm-high cylinder capacitor.

For 70nm generation, target EOT must be below 2.0nm, or otherwise the height of cylinder becomes unacceptably high. MIM structure seems to the solution for this target value. Recently, TiN/HfO_2/TiN structure has been reported as a promising candidate for such application [11]. EOT of 1.4nm with reasonable leakage current at 1fA/cell (@1.2V) has been achieved with this structure. Also this structure is thermally stable up to 550°C and its immunity against deoxidization during forming gas annealing, which has been a

issue in Ru/BST/Ru structure, has been obtained. Because of its logic-friendly low temperature process, MIM capacitor cell is suited for embedded-DRAM application. MIM capacitor cells with Ta_2O_5, Al_2O_3 and HfO_2 have been reported for embedded-DRAM products [12-14].

Even in trench-type cell, Al_2O_3 has been applied to capacitor dielectric [15]. This recent shift toward high-k dielectric seems inevitable regardless of cell structure.

Most of the recently reported high-k dielectric films are formed by ALD. Layer-by-layer deposition of ALD has an advantage of low defect density over conventional deposition technique and it provides excellent electrical property. Meanwhile according to its chemical reaction principle, deposition rate of ALD is relatively slow. Not only chip performance but also cost is an important factor in DRAM business. Therefore, this throughput issue might be critical in DRAM mass production. Semi-batch type ALD equipment has been proposed and it is expected to solve the problem.

Changing capacitor dielectric material is a risk factor, because it strongly affects yield and reliability of the DRAM products. Therefore, careful evaluation is necessary. MIS-Ta_2O_5, for instance, took more than ten years to be used in mass production since it first applied to DRAM. Establishing the evaluation method and criteria for capacitor reliability could be a long-term issue. MIM capacitor with exotic dielectric film may take some time to be employed in mass production stage. From above considerations, the use of MIS AHO could be extended down to 80nm generation, while beyond 70nm generation, MIM structure with HfO_2 (or other high-k dielectric, perhaps) is expected to replace MIS technology.

III. GATE DIELECTRIC MATERIALS

3.1. SiON for gate dielectric

Trend of supply voltage and gate SiO_2 thickness in DRAM products is summarized in Fig. 4. SiO_2 has been used as a gate dielectric material since the birth of DRAM according to its excellent reliability and SiO_2/Si interface properties. Also high process temperature required for capacitor formation and high cost avoided the employment of surface-channel PMOSFET into commodity DRAM process. Therefore, buried-channel PMOSFET, accordingly the gate SiO_2, has been used for a very long time. However, as the design rule reaches sub-100nm regime, gate length in periphery circuit region becomes below 200nm and controlling the short channel effect of buried channel PMOSFET is becoming a critical issue. In addition, request for reducing threshold voltage Vt and subthreshold swing of PMOSFET is rising in order to meet device requirements for low power application. Furthermore, thermal budget to form storage capacitor is reduced by the introduction of high-k material. Hence, surface-channel PMOSFET and gate SiON have been applied to commodity DRAM products [16]. Various methods to form gate SiON, for example NO annealing [17], plasma nitridation [18] and ALD [19], have been proposed. Like logic products, thin EOT, low gate leakage, excellent immunity against boron penetration and high reliability is required. For DRAM application, interface state increase and process-induced damage during nitridation must be suppressed to avoid anomalous leakage in memory cell in order to achieve sufficient data retention characteristics.

Applying gate SiON to DRAM seems to have great impact on data retention characteristics. Because increasing permittivity of gate dielectric makes Vt of memory cell transistors lower. Figure 5 shows nitrogen concentration dependence of Vt. Vt decreases as the peak concentration becomes higher and Vt lowering of 0.15V has been observed at 10% nitrogen concentration. Vt of memory cell transistor must be kept high enough to minimize the subthreshold leakage current in memory cell. In order to keep Vt at certain level, substrate-doping concentration must be increased to compensate the Vt lowering caused by EOT decrease. Such approach will consequently increases electric field in memory cell and degrades data retention characteristics. Therefore, structure of the cell transistor must also be taken into account to solve the problem. Recessed Channel Array Transistor (RCAT) [20], P^+-gate NMOS memory cell transistor [21] and negative wordline scheme [22] have been proposed for electric-field relaxation (Fig. 6). Gate SiON film will be incorporated with these novel cell transistors.

3.2 Other high-k gate dielectric materials

In DRAM, transistors with minimum gate length are used in memory cell array. To ensure writing "high" data to the storage capacitor, gate voltage Vg must be boosted up to Vt+Vd during the write operation. Therefore, gate dielectric film thickness of memory cell transistors is designed to be thicker than that of periphery circuit transistors. Meanwhile gate length of transistors in peripheral circuit region is expected to be around 100nm even in 70nm technology node. Therefore, gate dielectric thickness of DRAM products is not aggressively scaled down as the logic devices. Trend of gate oxide thickness also insists that gate SiON provides sufficient EOT down to 60nm generation (Fig. 4). Introduction of high-k gate dielectric film, such as HfO_2, to commodity DRAM products might be delayed from above considerations.

IV. INTER-LAYER DIELECTRIC MATERIALS

Schematic drawing of sub-100nm DRAM cell structure is shown in Fig. 7. Ever since Shallow Trench Isolation (STI) replaced LOCOS for device isolation technology, High Density Plasma (HDP)-CVD oxide has been widely used as trench filling material according to its excellent gap-filling property [23]. As the scaling continues below 100nm, however, aspect ratio of STI well exceeds the HDP gap-filling capability. Therefore several process refinements were proposed to overcome such problem. Poly-Si is known to have superior gap filling capability and it is proposed to replace HDP SiO_2 as a trench filling material [24]. Another approach to achieve void-free gap filling is to use Spin-On-Glass (SOG) pillar at the trench bottom [25]. This HDP/SOG bi-layer gap filling also reduces mechanical stress at the STI top corner and thus improves device performance such as hot carrier immunity and data retention characteristics.

Inter-wordline and inter-bitline gap filling is also becoming a critical issue in sub-100nm generation. Increasing boron/phosphorus concentration or utilizing steam-reflow process has extended the use of BPSG as an ILD material. However, its gap-filling capability is approaching its limit and demand for low-temperature gap-fill process forces to make transition to other ILD materials. Recent work has shown that SOG film is capable of filling high-aspect ratio inter-wordline gap [26].

ILD material has great impact on device performance as well. It is well known that

moisture in BPSG and other ILD materials causes hump in I-V curve of transistors [27, 28]. In order to overcome this issue, blanket Si_3N_4 diffusion barrier layer is indispensable. Therefore, 1ILD still needs to be SiO_2/Si_3N_4 bi-layered

In order to minimize cell size, misalignment tolerance between wordline (or bitline) and contact is extremely small in DRAM cell. Self-Aligned Contact (SAC) process has been introduced as the solution to realize alignment-margin-free $8F^2$ cell from 0.2μm generation. Wordlines (or bitlines) are surrounded by Si_3N_4 to prevent short circuit between the wiring. However, as the wiring pitch becomes tighter, spacer Si_3N_4 thickness must be thinner to provide space for contact and wordline. Since it seems quite difficult to improve selectivity of the contact etching, novel dielectric material with superior etching selectivity to SiO_2 is needed in order to extend this technology down to sub-100nm regime.

V. SUMMARY

The requirements, integration issues and recent advances in capacitor, gate and ILD for sub-100nm DRAM have been discussed. To obtain storage capacitance of 30fF/cell, target equivalent oxide thickness must be scaled down to 1.75nm in 70nm DRAM technology node. MIM capacitor with high-k dielectric would be indispensable for this generation. In case of gate dielectric, both NMOS and PMOSFETs will be surface-channel transistors and, therefore, gate SiON film will be gradually introduced from 90nm DRAM technology. To achieve void-free gap filling, SOG film will play an important role as an ILD material for sub-100nm DRAM. Continuous effort to search for novel dielectric material is needed to overcome scaling issues. Establishing reliability evaluation method and criteria could be a long-term issue.

REFERENCES

[1] M. Sakao et al., IEDM Tech. Dig., p.655-658 (1990).
[2] G. T. Jeong et al., IEEE Trans. on Electron Devices, Vol.44, No.11, p.2064-2069 (1997).
[3] I. S. Park et al., Symp. on VLSI Tech., p.42-43 (2000).
[4] T. Rupp et al., IEDM Tech. Dig., p.33-36 (1999).
[5] M. Gutsche et al., IEDM Tech. Dig., p.411-414 (2001).
[6] K. Ono et al., IEDM Tech., Dig., p.803-806 (1998).
[7] S. Yamamichi et al., IEDM Tech. Dig.,p.119-122 (1995).
[8] J. Nakahira et al., Symp. on VLSI Tech., p. 104–105 (2000).
[9] P. -Y. Lesaicherre et al., IEDM Tech. Dig., p.831-834 (1994).
[10] J. H. Lee et al., IEDM Tech. Dig., p.221–224 (2002).
[11] J. H. Choi et al., IEDM Tech. Dig., p.661-664 (2003).
[12] S. Arai et al., IEDM Tech. Dig. , 18.3.1-18.3.4 (2001).
[13] F. Fishburn et al., Symp. on VLSI Tech., p.75-76 (2003).
[14] Y. Aoki et al., IEDM Tech. Dig., p.831-834 (2002).
[15] H. Seidl et al., IEDM Tech. Dig., p.839-842 (2002).
[16] Y. Hiura et al., IEDM Tech. Dig., p.389-392 (1998).
[17] B. Maiti et al., IEDM Tech. Dig., p.651-654 (1997).

[18] H. Yang et al., IEDM Tech. Dig., p.245-248 (1999).
[19] A. Nakajima et al., IEDM Tech. Dig., p.657-660 (2003).
[20] J. Y. Kim et al., Symp. on VLSI Tech., p.11-12 (2003).
[21] K. Saino et al., IEDM Tech. Dig., p.415-418 (2003).
[22] N. Kasai, VLSI Technology Short Course (1998).
[23] M. Nandakumar et al., IEDM Tech. Dig., p.133-136 (1998).
[24] Y. Park et al., IEDM Tech. Dig., p.391-394 (2002).
[25] J. H. Heo et al., Symp. on VLSI Tech., p.132-133 (2002).
[26] Y. K. Park et al., IEDM Tech. Dig., p.819-822 (2002).
[27] I. G. Kim et al., IEDM Tech. Dig., p.827-830 (2002).
[28] S. K. Park et al., Proc. Int. Reliab. Phys. Symp., p.164-168 (2000).
[29] J. W. Kim et al., IEDM Tech. Dig., p.793-796 (1999).
[30] S. H. Oh et al., Symp. on VLSI Tech., p.73-74 (2003).
[31] J. M. Park et al., IEDM Tech. Dig., p.823-826 (2002).
[32] W. D. Kim et al., Symp. on VLSI Tech., p. 100-101 (2000).
[33] J. H. Lee et al., Symp. on VLSI Tech., p.114-115 (2002).

CY		1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004
Conference	Bit density	1M		4M	16M				64M		256M		1G		1G/4G							
Conference	Design rule [um]	1.6	1.0	1.0	0.7	0.5			0.4		0.25		0.16	0.15			0.14	0.13/ 0.11		0.09	0.08	0.07
Mass production	Bit density 16K																					
Mass production	Bit density 64K	64K																				
Mass production	Bit density 256K					256K																
Mass production	Bit density 1M		ES						1M													
Mass production	Bit density 4M					ES							4M									
Mass production	Bit density 16M								ES						16M							
Mass production	Bit density 64M											ES						64M				
Mass production	Bit density 128M																		128M			
Mass production	Bit density 256M													ES								256M
Mass production	Bit density 512M																		ES			
Mass production	Bit density 1G																				ES	
Mass production	Design rule [um]				1.20	1.00	0.80	0.70		0.63	0.45	0.56	0.40	0.36	0.28/ 0.25	0.22	0.20/ 0.18	0.15	0.13		0.11	
Mass production	Cell structure		Planar											Trench								
										Stack												
													FIN									
												COB(Box)										
															Box+HSG							
																			Concave+HSG			
																			Cylinder			
																		Cylinder+HSG				
Mass production	Capacitor dielectric material				ONO									NO								
																				Ta2O5		
																					Al2O3	
Mass production	Cs [fF/cell]											30+/-5										
Mass production	Gate dielectric material											SiO2										
Mass production	Gate Tox [nm]	47.0	35.0		22.0	20.0			18.0			14.0		11.0	10.0	9.0	8.0	7.0	4.2		3.6	
Mass production	Vdd [V]					5.0									3.3				2.5		1.8	
Mass production	Isolation dielectric material								LOCOS (Thermal oxide)													
																			STI (TEOSNSG/HDP)			
Mass production	ILD material									BPSG reflow										BPSG steam reflow		

Fig. 1. Evolution of cell structure and dielectric material in DRAM products.

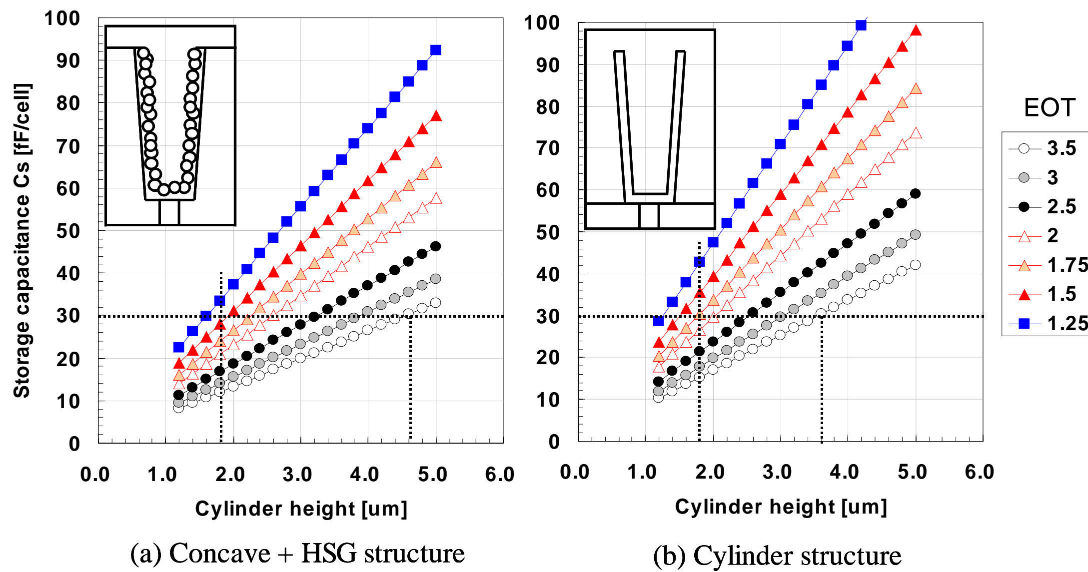
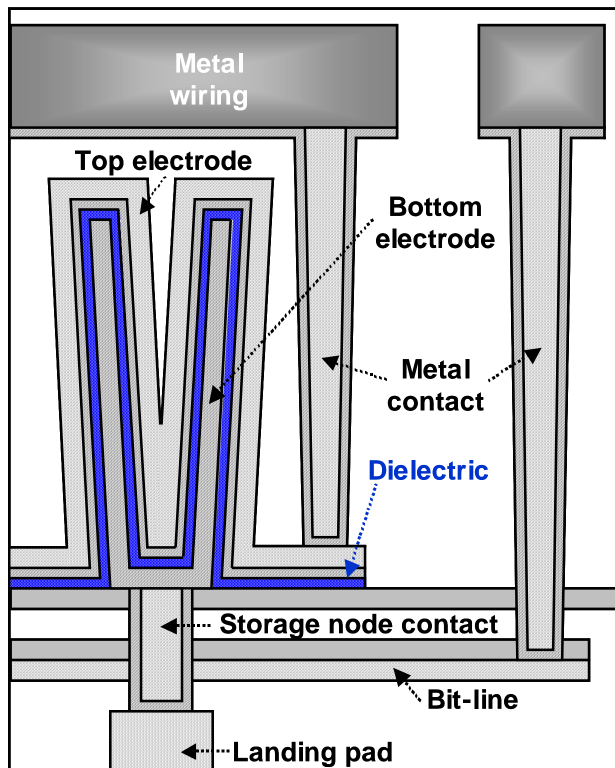


Fig. 2. Estimated storage capacitance for 70nm technology. (a) Concave +HSG structure, (b) Cylinder structure.



Requirements for sub-100nm DRAM capacitor dielectric

- High-k
- Low leakage
- Small temperature dependence
- High reliability
- Excellent step coverage
- Thermally stable
- Good electrode affinity
- No hysterisys
- Excellent controllability
- Thin electrode
- Forming gas immunity
- Small capacitance loss

Fig. 3. Requirements for sub-100nm DRAM capacitor dielectric.

Table 1. Recent reports on high-k capacitor dielectric.

	Cell structure	Material	EOT	Ileak	Cs	Cylinder height (or Trench depth)	Reference
MIM	Stack (Box)	Ru/(Ba, Sr)TiO3/Ru	0.8nm	<1E-7A/cm2(@1V)	25fF/cell(@F140nm)	0.2um	[6]
MIM	Stack (Concave)	Ru/SrTiO3/Ru	0.53nm	10fA/cell(@0.8V)	NA	0.55um	[5]
MIM	Stack (Planar)	Ru/Ta2O5/Ru	0.8nm	<1E-7A/cm2(@1V)	NA	NA	[29]
MIM	Stack (Cylinder)	TiN/HfO2/TiN	1.4nm	1fA/cell(@1.2V)	40fF/cell(@F090nm)	1.4um	[11]
MIM	Stack (Cylinder)	TiN/HfO2/TiN	1.3nm	<1E-7A/cm2(@1V)	NA	NA	[30]
MIM	Stack (Cylinder)	TiN/Al2O3/TiN	NA	0.6fA/cell	26fF/cell(@F110nm)	NA	[13]
MIM	Stack (Cylinder)	TiN/AHO/TiN	1.5nm	<1fA/cell(@1.2V)	40fF/cell(@F088nm)	1.5um	[31]
MIM	Stack (Concave)	W/TiN/HfO2/TiN	1.2nm	<0.01fA/cell(@1.0V)	15.5fF/cell(@130nm e-DRAM)	0.4um	[14]
MIM	Stack (Concave)	W/TiN/Ta2O5/TiN	1.5nm	10fA/cell(@1V)	20fF/cell(@130nm e-DRAM)	NA	[12]
MIM	Stack (Cylinder)	Ru/Ta2O5/TiN	1.8nm	0.1fA/cell(@1V)	40fF/cell(F130nm)	1.0um	[32]
MIS	Stack (Cylinder)	TiN/AHO/poly	2.1nm	1fA/cell(@1.75V)	-	1.3um?	[33]
MIS	Stack (Cylinder)	TiN/AHO/poly	2.25nm	1fA/cell(@1.65V)	27.7fF/cell equivqlent	A/R>40	[10]
SIS	Trench	poly/Al2O3/poly	NA	0.1fA/cell(@1V)	36fF/cell(@F110nm)	NA	[15]

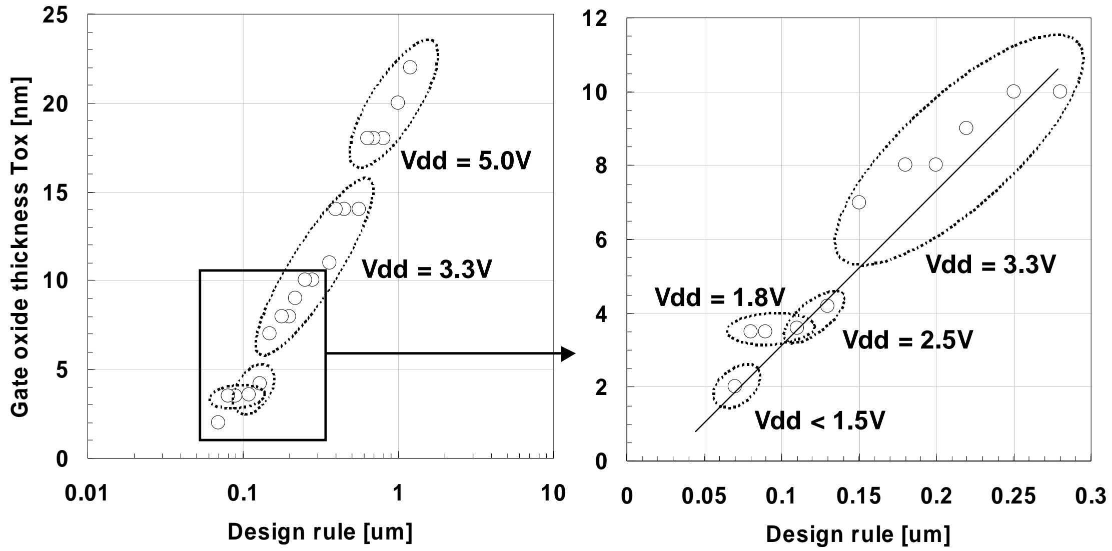


Fig. 4. Trend of supply voltage Vdd and gate oxide thickness in DRAM products.

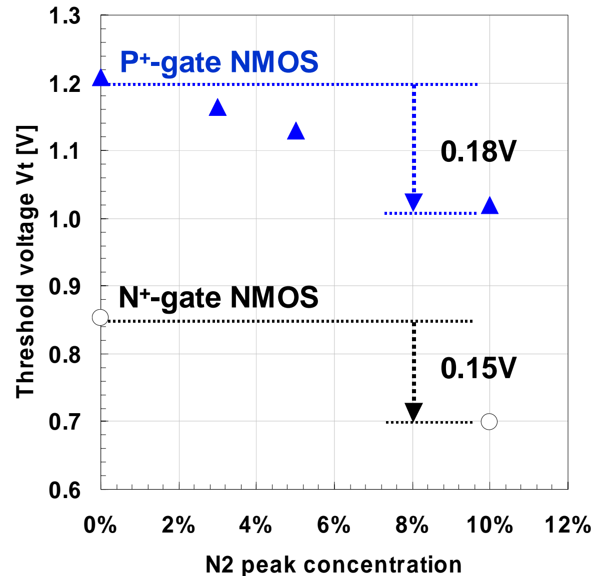


Fig. 5. Impact of gate SiON N_2 peak concentration on the Vt of memory cell transistor.

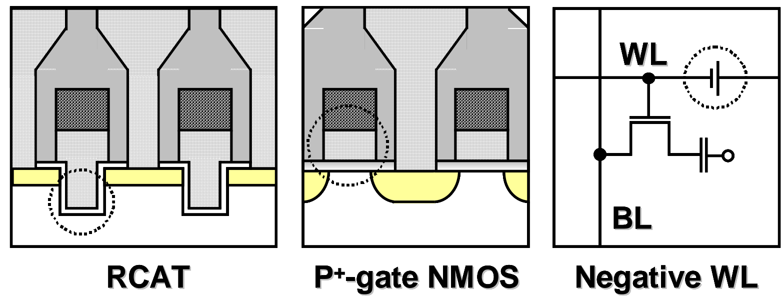


Fig. 6. Candidates for sub-100nm DRAM cell transistor.

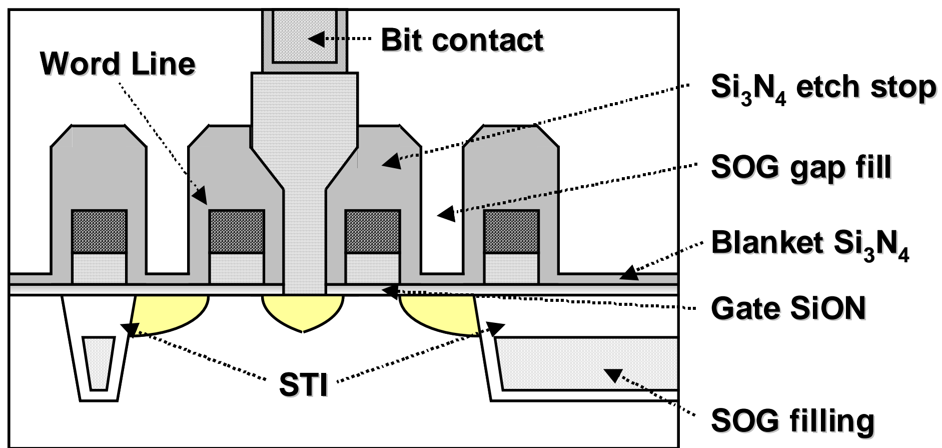


Fig. 7. Schematic drawing of sub-100nm DRAM cell structure.