

### Low-k Dielectrics

#### For DRAM Frontend-Of-Line And Mid-Of-Line

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Advanced low-k technologies are rapidly approaching production maturity for logic and most recently DRAM products. For the sub-70 nm DRAM generations, optimization of RC delays for fast signal transfer as well as reduction of parasitic capacitance is attracting the attention of designers as well as integration engineers. However, it is not only the classical topics such as these can be addressed with the help of low-k materials. The need for void-free gapfill materials also provides a large field of play for low-k materials, where they can be used in a sacrificial as well as a permanent way. We have investigated different approaches to processing low-k's in DRAM production flows. The purely organic SiLK™ S was found to provide excellent process selectivity and sufficient temperature stability for the subsequent deposition of oxide liners, etc., thus enabling completely new integration scenarios in structures of aspect ratios up to 70. The low-k flowfill™ (k=2.8) /1/ process was employed as a permanent low-k inter-wordline fill for vertical transistors of future DRAM generations. Local planarization behavior of low-k flowfill is good enough to overcome the need of additional CMP. With the same material used as M0 inter-metal dielectric, the parasitic bitline-to-bitline coupling could be reduced by 15% compared to a state-of-the-art 90 nm DRAM process.

### INTRODUCTION

In addition to a low dielectric constant, many low-k material processes exhibit excellent gapfill behavior because they are mostly deposited as liquids (e.g. spin-on, CVD condensation processes). Such a property makes low-k very attractive for high-aspect-ratio structures if temporary /2/ or permanent fill functions have to be addressed. Of special interest is the combination of sacrificial fill materials with deposition and etch processes of Si, SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub>. Such a challenging approach, which is limited by the T<sub>g</sub>=490°C of Dow Chemical's SiLK™ S, is shown in this paper. Furthermore, it is illustrated how Trikon's low-k flowfill™ can be permanently integrated into a future DRAM array device structure, targeting not just the benefit of electrical coupling, but also for the extraordinary fill behavior, reduced stress compared to pure SiO<sub>2</sub> fill, and temperature stability to beyond 1100°C/100 sec - i.e. withstanding more than the typical thermal budget of a future DRAM production flow without forcing delamination of encapsulation layers. We have also gained preliminary results for the integration of low-k flowfill in combination with a CVD oxide capping layer as inter-metal dielectric (IMD) in the bitline layer (M0). We targeted the reduction of the bitline capacitance as well as the inter-bitline coupling by substituting the inter-M0 oxide by a locally self-planarizing low-k material.

### EXPERIMENTAL

Sacrificial low-k in the DRAM deep-trench module was employed to integrate a DRAM deep trench /3/

capacitance enhancement method such as Hemispherical Grained Silicon (HSG) /4/. Among several material options, SiLK S /5/ proved to be beneficial for void-free gap fill and selectivity for etching and stripping as well as thermal stability, thereby enabling the direct deposition of an oxide liner, for example.

Low-k as fill material of surrounding-gate vertical transistor arrays /6/ was integrated in a DRAM production flow. After formation of the active trench (AT) and the surrounding wordline, the space between the wordlines has to be sealed with dielectric material that exhibits good gap fill capability and very high thermal stability as well as a low dielectric constant. For this purpose, Trikon's CVD condensation process was tested, which is based on methyl-silane and gaseous peroxide.

The read/write signal of DRAM cells strongly depends on the relation of bitline-capacitance to the capacitance of the storage capacitor, independent of trench or stacked cell concepts. The lower the bitline capacitance the more voltage shift is achieved by connecting a given storage capacitor owning charge +/-Q to the bitline by activating the gate of the corresponding array device. As a consequence, integrating low-k materials in-between the bitlines is highly desirable.

### CONCLUSION

We have shown three different approaches that use or integrate low-k materials in deep-trench based DRAM FEOL and MOL and as an extension of the classical approaches in BEOL. In general, integration schemes based low-k materials facilitate the development of future DRAM generations in various ways and help support the DRAM shrink roadmap.

### ACKNOWLEDGEMENTS

We gratefully acknowledge technological support by K.L. Foster and team of Dow Chemical and by Trikon Technologies. We also want to thank Infineon's low-k development team: J. Amon, J. Bachmann, L. Bauch, A. Feicke, S. Finsterbusch, T. Gärtner, J. Hahn, T. Hingst, U. Kirbach, S. Kundalgoruki, K. Mai, M. Markert, C. Messerschmidt, H. Neef, M. Nichterwitz, H. Rettenmaier, U. Ritter, U. Scheler, J. Schulze, K. Schupke, H. Steinmetz, U. Strohbach, S. Strube, A. Thamm, R. Trinowitz, N. Urbansky, K. Zimmermann, and E. Zoch.

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