Extending the Reliability of SiO_2-Based Dielectric to the Nanometer Limit

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ABSTRACT –
The limitations of silicon dioxide dielectric reliability for future CMOS scaling are investigated. Several critical aspects are examined, and new experimental results are used to form an empirical approach to a theoretical framework upon which the data is then interpreted. Experimental data over a wide range of oxide thickness, voltage, and temperature were gathered using structures with a wide range of gate-oxide areas, and over very long stress times. Resolution of seemingly contradictory observations regarding the temperature dependence of oxide breakdown is provided by this work. On the basis of these results, a unified, global picture of oxide breakdown is constructed and the resulting model is applied to project reliability limits for the wear-out of silicon dioxide. It is concluded that silicon dioxide-based dielectrics can provide reliable gate dielectric, even to a thickness of 1nm, and that CMOS scaling may well be viable to the 50 nm technology node using silicon-dioxide-based gate insulators.

Keywords- Dielectric Breakdown, Reliability Methodology, MOS Devices, Ultra-Thin Gate Oxide.