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HOT CARRIER STRESS AND BREAKDOWN IMPACT ON HIGH-FREQUENCY MOSFET ANALOG PERFORMANCE

Luigi Pantisano, #D.Schreurs, B.Kaczer, E.Simoen and #G.Groeseneken

IMEC Kapeldreef 75 Leuven B-3001 Belgium,
#KU Leuven, Email luigi.pantisano@imec.be

RFCMOS has become a viable, cost-effective solution for applications in the GHz range [1]. In the past few papers were published on the impact of hot carrier stress [2-5] and breakdown on RF devices [6,7] for thick oxide technologies. Analog devices feature a broad choice of possible bias (V_G, V_D). In this paper an in-depth analysis of the impact of Hot Carrier Stress (HCS) and Gate Oxide Breakdown (GOX BD) on 90nm RFCMOS technology, especially under the low V_G/high V_D bias condition. Analog devices are highly vulnerable to HCS under this condition (see fig.1). Fundamental RF parameters like f_T and f_{Max} are proportional to G_m. At conference time it will be shown that several important factors have to be taken into account to properly evaluate the impact of hot carrier stress and breakdown on the analog performance of the 90nm RFCMOS devices. The RF-performance decrease after HCS is more pronounced at bias operation close to V_{TH}. In the case of the analog devices the HC-lifetime is worse than the digital ones due to the "duty-cycle for stress" effect. Moreover the impact on the RF performances also depends on the device length.

Furthermore, at the low-V_G and high-V_D bias condition, the HCS increases the probability of a gate-to-drain (GD) BD over a gate-to-source (GS) or a gate-to-substrate BD [8]. Conversely from previously reported experiments [6,7], in this experiment a single drain (source) BD path was carefully obtained. (The technique is demonstrated in ref. 9). The breakdown spot is treated as a resistance connected between gate and the source (drain) terminal thus effectively extending the model already demonstrated for DC characteristics [9]. The BD spot impedance R_{BD} can be extracted from DC measurement using $R_{BD}=\Delta I_G/\Delta V_G$. For each bias condition, after breakdown the RF response of a BD path can be "deembedded" from the fresh samples by using

$$Y_{BD}^{Drain,Source} = Y_{BD} - Y_{FRESH} \qquad \text{(eq.1)}$$

The admittance parameters are very different in the case of Gate-to-Source (eq.3) and Gate-to- Drain BD (eq.4). Fig.2 shows the Y-parameters measured in accumulation (V_G=-1.5V, V_D=0V). The asymmetry after BD (GS or GD) induces an asymmetry in the Y-parameters (Fig.10). Gate-to-source BD induces a change only in Y_{11} (=$\Delta I_G/\Delta V_G$) while all Y-parameters are affected for BD between the gate and the drain contacts. A BD path induces a change only in the real part of Y-parameters, consistent with the resistive (dissipative) contribution picture [8]. No measurable change in the imaginary part was observed, within the instrument and deembedding model limit. The real part of Y_{11} extending from DC to 5GHz, thus serves as a measure of the BD resistance. Values very close to the ones measured at DC conditions are indeed found.

The GOX breakdown occurrence can have a devastating effect on input and output mismatch as well as MOSFET gain. A model will be proposed to quantify the effect of GOX BD on the RF parameters taking into account the BD resistance and the path position. This model has been verified for small and large signal operations. The effect on GOX BD on the low frequency noise seems not as devastating as the I/O mismatch.

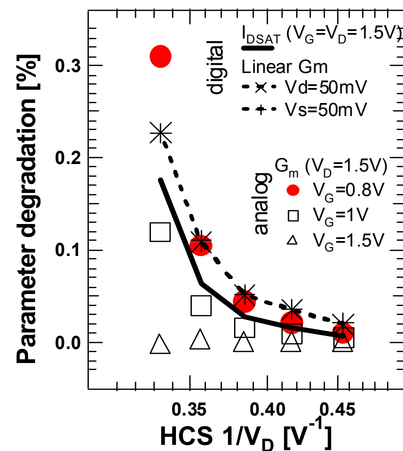

Fig.1: Analog devices feature a broad choice of possible bias, depending on the application considered. Hot carrier Lifetime for digital devices is routinely done under worst-case condition. However the choice of bias for the analog ones is much broader. In order to compare digital and analog devices, a single worst-case scenario has been chosen (100s stress time). After maximum substrate HC stress, the worst-case degradation of a device under "digital bias" (I_{DSAT} @ V_G=V_D=1.5V, peak G_m) can be close to the "analog bias"(i.e., V_G~V_{TH}, V_D=1.5V).

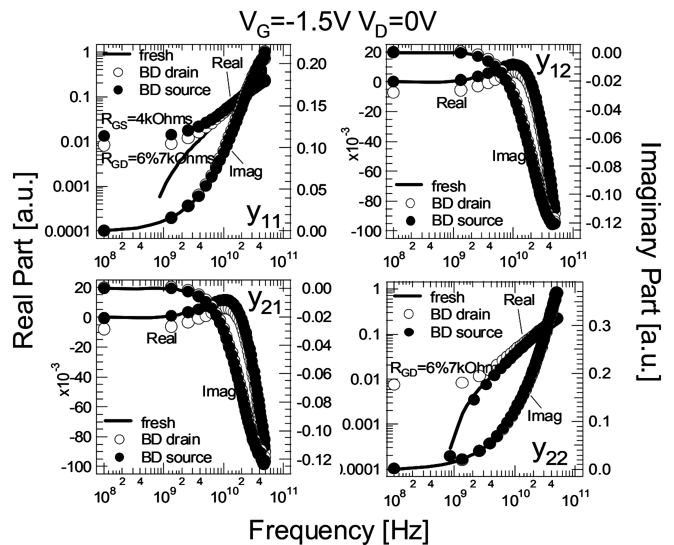

Fig.2: Comparison between fresh and broken devices in accumulation (V_G=-1.5V, V_D=0V). At DC the breakdown resistance is R_{GD}=7kΩ, while R_{GS}=5.3kΩ. These values are very close to the ones measured with the Y-parameters. The gate-to-source breakdown modifies only Y_{11}, while all Y's are affected by the gate-to-drain breakdown. Only the real part of Y-parameters is affected, thus confirming that the breakdown path behaves like a resistor (i.e., dissipates power) up to 5GHz.

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