SOI CMOS CIRCUITS FOR SYSTEM-ON-CHIP (SoC) APPLICATION

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This paper presents Silicon-on-Insulator (SOI) CMOS RF integrated circuits for SoC application. It covers from the SOI CMOS technology and the integration of high-performance passive devices to RF circuits design. We show that the ability of SOI NMOS transistors to function as high-bandwidth amplifiers continuously improves as gate length shrinks below 50nm. F_T of 196GHz is achieved at Lpoly = 47nm. We also present four features of an aggressively scaled 120nm partially-depleted SOI CMOS technology that show its suitability for high-frequency circuit applications as compared to bulk CMOS and III-V technologies. A symmetrical STP (single-turn and multiple metal levels in parallel) inductor exhibits a Q of 52, by a High-Resistivity Substrate (HRS) and an inductance density of 5302 fH/μm² is achieved for a 42nH MTS (Multi-turn, multiple metal layers in Series) inductor. The capacitance density of the Vertical Native Capacitor (VNCAP) in a 90nm SOI CMOS improves by 28%, without any extra cost due to the scalability of the metal pitches as compared to a 120 nm SOI CMOS. A capacitance density of 1.8fF/μm² is obtained for only 6 metal layers. Also, a quality-factor of 105 at 4GHz is measured for a 1pF VNCAP. Four 5GHz LC-tank VCOs were fabricated, the measured frequency tuning range is 22% and the phase noise is -126dBc/Hz at 1MHz offset of the 4.5GHz carrier. Oscillation was achieved at 5.4GHz at a minimum power consumption of 500μW. The 40-50 GHz VCOs for embedded RF integrated circuits exhibits wide tuning range, which is a key aspect of VCO manufacturability. We achieved up to 15% frequency tuning range from 43.5 to 50.5GHz and -90.2dBc/Hz phase noise performance at 1 MHz offset from 50.1GHz operating frequency. The total power dissipation is 15mW at 1.8V. A 9-stage distributed amplifier exhibits a gain of 11dB with a 90GHz 3dB cut-off frequency is measured, which is equivalent to a 320GHz gain bandwidth product (GBW). The measured 1dB output compression point (P1dB) is 12dBm at 20GHz, the output IP3 (OIP3) is 15.5dBm at 50GHz, and the noise figure is 5.5dB at 18GHz. A 2:1 static frequency divider exhibits a maximum operating frequency of 33GHz.

For the system-on-chip application, this paper demonstrated manufacturable RF integrated circuits fabricated in SOI CMOS technology with a RFIC design flow. To fulfill circuit specifications fairly, designers have to make out all design procedures from the selection of a suitable technology to accurate data analysis. Most outstanding results described in this paper could not be reproduced without full of technology understanding. We have also investigated the potential of the SOI technology through the process regime, the device performance and the circuit level. For the first time high-performance manufacturable RF circuits can be integrated in a standard SOI CMOS technology.

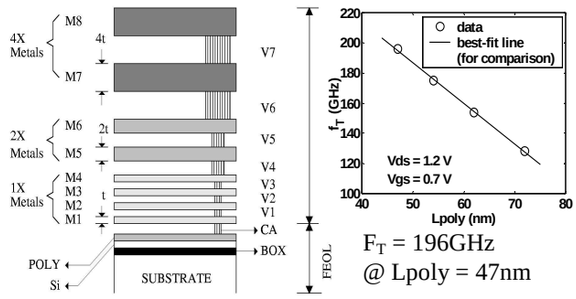

Figure 1 A SOI CMOS cross-section (Technology)

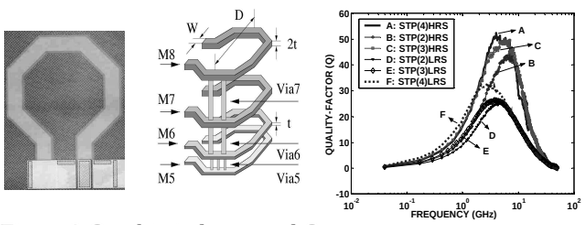

Figure 2 On-chip inductor and Q measurement

Tech.	BEOL	Metal Pitch	Capacitance Density	Δ (%)
120nm	1x, 2x	200nm	1.40fF/μm²	-
90nm	1x, 2x	140nm	1.80fF/μm²	28%
***** Estimation for 65nm CMOS technology**				
65nm	1x, 2x	90nm	2.20fF/μm²	57%

Table 1 VNCAP capacitance density

[Ref]	Tech	FTR (%)	Phase Noise (dBc/Hz)
[30]	CMOS	6%	-90.5
[31]	Bipolar	7%	-95.5
[32]	SiGe	12%	-118
[33]	CMOS	7%	-101
[34]	SiGe	3%	-103
[35]	CMOS	4%	-110
[36]	CMOS	18%	-114
Present	SOI	22%	-119

Table 2 5GHz VCO phase noise and FTR

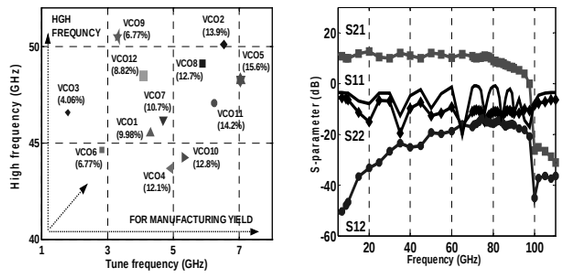

Figure 3 50GHz VCO result and 320GHz GBW DA

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