HfSiON GATE DIELECTRICS FOR LOW-STAND-BY POWER CMOS DEVICES

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HfSiON film is considered to be a promising candidate for alternative gate dielectrics because of its good interface properties and sufficient thermal stability for integration with conventional poly-Si gate CMOS fabrication process [1][2]. However, there are still some issues (carrier mobility, ΔVfb, reliability) to be overcome in order to make HfSiON with conventional poly-Si gate CMOS devices manufacturable. In this paper, we review our resent results concerning poly-Si/HfSiON gate stack for low-stand-by power (LSTP) CMOS device fabricated by conventional poly-Si gate process. We discuss the ΔVfb problem of poly-Si/HfSiON gate stack, the way to improve effective carrier mobility by nitrogen profile engineering, and breakdown mechanism of HfSiON film.

Fig.1 shows C-V characteristics of nMOS capacitors with n^+- and p^+-poly-Si gate electrode. In this case, about +200 mV shift and -600 mV shift are observed for n^+- and p^+-poly-Si, respectively. The shifts in the opposite directions for n^+- and p^+-poly-Si indicate that the main origin of ΔVfb is not fixed charge in the film. Vth control of poly-Si/HfSiO gate stack has succeeded by channel engineering for LSTP CMOS device [5]. Understanding the origin of ΔVfb and creating the solution of Vth control is required.

Fig.2 demonstrates that carrier mobility of thermal nitrided (TN) HfSiON degrades as nitrogen concentration increases, while the degradation of carrier mobility in both nMOS and pMOS can be suppressed by plasma nitrided (PN) film. High carrier mobility can be obtained while keeping sufficient thermal stability and resistance to boron penetration by PN. **Fig.3** shows gate leakage current of nMOS capacitors with PN and TN HfSiON gate dielectrics measured at |Vfb-1| V as a function of EOT. The gate leakage current of PN HfSiON is about one order of magnitude lower (about 4 orders of magnitude lower than that of SiO_2) than that of TN HfSiON at the same EOT. Nitrogen profile engineering in HfSiON has much advantage for obtaining not only higher carrier mobility but also thinner EOT and lower gate leakage current.

In **Fig. 4**, the relationship between N_{BD} and physical thickness is shown. N_{BD} of HfSiO is smaller than the reference SiO_2 value, indicating the weak film property against stress for HfSiO. This weakness could be due to larger effective defect size and existence of large amount of defects exists in initially. N_{BD} of HfSiON exhibited larger value, indicating that introduction of nitrogen into HfSiO is important in terms of reliability.

In this paper, we have reviewed our recent results of poly-Si/HfSiON gate stack for LSTP CMOS device. Incorporation of nitrogen is important from the viewpoint of reliability as well as thermal stability. Nitrogen profile engineering in HfSiON has much advantage for obtaining not only higher carrier mobility but also thinner EOT and lower gate leakage current. Although Vth control for LSTP device has succeeded by channel engineering, more study to understand the origin of ΔVfb is required to solve the problems. More work is required to understand breakdown mechanism of HfSiON film and establish a model for life time projection.

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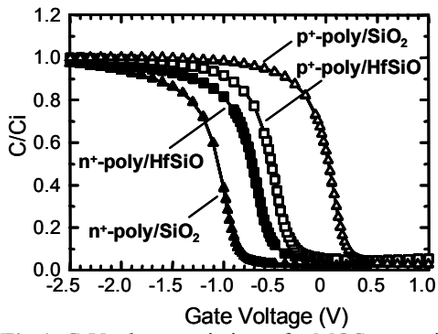

Fig.1 C-V characteristics of nMOS capacitors with n+-poly-Si and p+- poly-Si gate electrode.

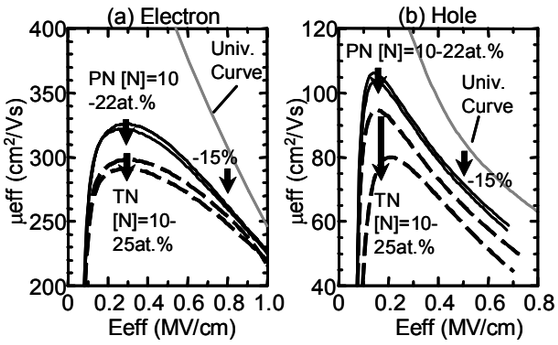

Fig.2 (a) Electron and (b) hole mobility of PN and TN HfSiON vs nitrogen concentration

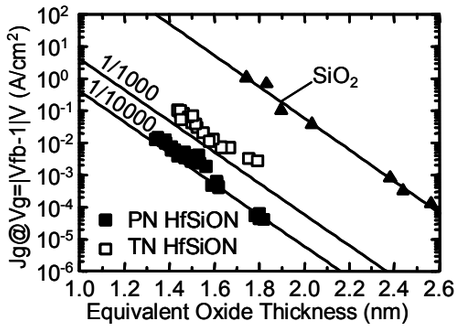

Fig.3 Summary of EOT-Jg relationship of HfSiON nitrided by PN and TN

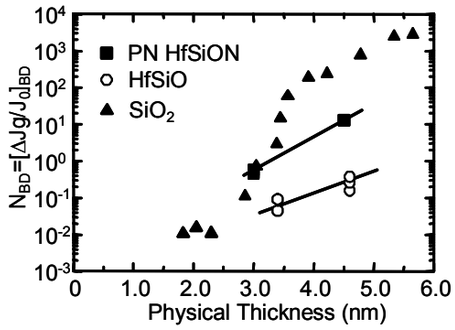

Fig.4 $N_{BD}([\Delta J/J_0]_{BD})$ vs. physical thickness