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ALD HfSiO high-k dielectrics for future CMOS

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In applications of high-k dielectrics to future CMOS devices, many challenges intensively focused on the interface of Si/high-k and high-k/gate electrode. However, the enhancement of intrinsic properties of high-k materials and thickness controllability are more important in scaling of CMOS. Among the methods to improve these requirements, atomic layer deposition (ALD) can be a good candidate. ALD method has advantages in thickness and composition uniformity and controllability over ultra-thin gate dielectric compare to chemical vapor deposition (CVD) counterpart.

As an alternative gate dielectric for sub-100nm MOSFETs, HfSiO has proven to be a promising high-k dielectric with lower diffusivity of impurities and improved channel mobility characteristics [1]. In the case of HfSiO, not many precursors for ALD have been reported yet [2], especially since SiO_2 layer does not grow in the temperature range where atomic layer deposition of HfO_2 occurs. However, we fabricated MOSFETs with HfSiO dielectric deposited by ALD method with Hf and Si liquid precursors. Using ALD method, it was found that digital control of dielectric thickness below 1nm was possible. Also, the Hf and Si concentration in HfSiO film is easily controlled by Hf/Si feed ratio. We concluded that that Jg-EOT characteristic was improved with higher Hf contents. Compared to SiO_2, HfSiO deposited by ALD showed 2 orders of Jg reduction with 25at% of Hf, and 3 orders of Jg reduction with 70at% of Hf. Finallly, the optimum performance of MOSFETs with ALD HfSiO is determined to be Hf concentration of about 33%.

With high-k dielectrics, metal gates will be the unique solution to eliminate gate depletion and other issues like boron penetration and fermi level pinning. Metal gates can be realized in gate-first or gate-last process. The main advantage of gate-last process is free from damage during gate stack integration process. But, its process is very complex. On the other hand, the gate-first process is more compatible with conventional poly gate process. However, there are some disadvantages such as difficulty of metal etching, integration of gate stack and contamination during post high temperature process. In order to use gate-first process, the thickness of metal gates should be as thin as possible.

A number of metals have been investigated as gate materials such as TiN [3], Mo [4], Ta, TaSixNy [5], NiSi [6]and TaN. Among these metals, CVD-TaN is considered as a promising candidate due to its excellent thermal stability and damage-free process in comparison to PVD-TaN. Our experimental results show that no gate depletion effect was observed with TaN gate. Detailed results will be discussed.

Reference

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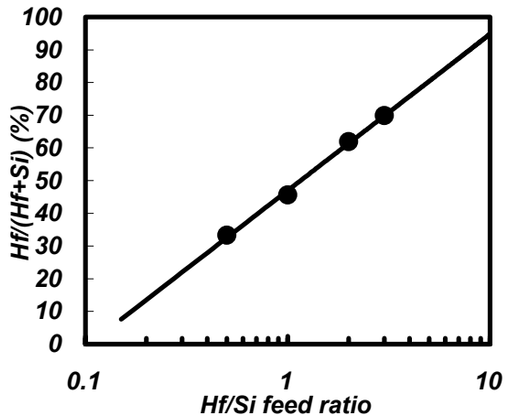

Fig. 1 Hf concentration in ALD HfSiO depending on Hf/Si feed ratio measured by x-ray photoelectron spectroscopy

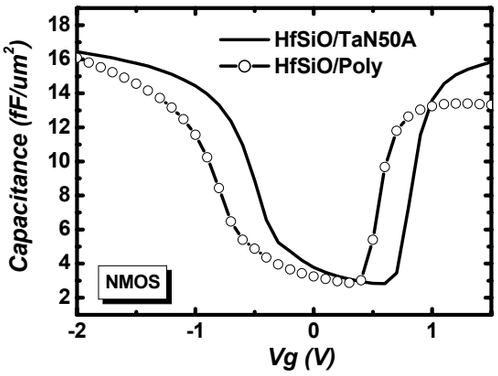

Fig. 2 C-V characteristics of nMOSFET with HfSiO gate dielectric. There is no gate depletion with 50Å CVD-TaN metal gate.