Atomic-Layer Deposition of Ultrathin Silicon Nitride for Sub-Tunneling Gate Dielectrics

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Low temperature growth of silicon nitride is one of the key technologies for the next generation gate dielectrics. Several methods have been proposed for such a growth [1,2]. Recently, we have developed an atomic-layer deposition (ALD) of silicon nitride [3]. The gate leakage current can be reduced due to the high dielectric constant of ALD silicon nitride [4]. Boron penetration can also be suppressed [3]. It has a superior control of film thickness and an excellent thickness uniformity especially in the thin region [3]. Also, the ALD silicon-nitride gate dielectrics have been found to be free from soft breakdown (SBD) phenomena [4,5], which are a severe problem in the progress of device scaling [6]. The SBD free phenomena are considered to be due to a reduced interface and bulk trap generations [7].

Recently, the post-stress mobility degradation of n-MOSFETs with ALD silicon-nitride gate dielectrics has been evaluated under the electron-injection by direct tunneling [8]. Though slightly smaller electron mobility for the ALD silicon nitride than for the reference SiO_2 was obtained in the fresh samples, electron mobility degradation was substantially reduced for the ALD silicon nitride. This is also considered to be due to the reduced interface and bulk trap generations for the ALD silicon-nitride gate dielectrics.

In this study, we confirm the superiority in the reliability of n-MOSFETs with ALD silicon-nitride gate dielectrics by evaluating the hot-carrier-induced V_{th} shift and discuss the applicability of the ALD silicon nitride to the next generation gate dielectrics.

I_d-V_d characteristics for the n-MOSFET with the ALD silicon-nitride (EOT=2.3nm) and SiO_2 (T_{ox}=1.8nm) gate dielectrics show clear saturation characteristics of the drain current. The channel length and the width are 1μm and 10μm, respectively. The V_{th} value is 0.46V for the SiO_2 and 0.44V for the silicon nitride extracted from I_d-V_g characteristics. The subthreshold slope is 100mV/dec for the silicon nitride and 80mV/dec for the SiO_2.

The value of the electron mobility (extracted from the I_d-V_g characteristics measured at V_d = 0.01V) for the ALD silicon nitride is smaller than that for the SiO_2. In the high effective normal field E_{eff} region, however, the difference becomes small. The mobility reduction may be ascribed to the effect of a long-range dipole field due to a larger ionic polarizability for silicon nitride than that for SiO_2 [9]. It could also be due to additional scattering by fixed charges in the silicon nitride [3].

Figure 1 shows the V_{th} shift after the hot carrier injection. The V_{th} shift is larger for the SiO_2 gate dielectrics than that for the silicon nitride ones at the same amount of carrier injection in the range from 10^{18} to 10^{21}electrons/cm^2. The reduced V_{th} shift for the ALD silicon nitride can be attributed to the smaller stress-induced bulk trap generations for the ALD samples than for the SiO_2 samples [7].

Taking the reduced gate leakage current [4], suppressed boron penetration [3], better TDDB characteristics [7], soft breakdown free phenomena [4,5], and reduced mobility degradation [8] for the silicon-nitride dielectrics into account, we believe that ALD silicon nitride is a very promising candidate to replace conventional SiO_2 dielectrics for sub-100-nm technology applications.

In addition, the proposed ALD silicon-nitride dielectrics can be applied to a thin barrier layer to suppress the formation of an interfacial layer having a low dielectric constant during the growth of high-*k* gate dielectrics such as ZrO_2 [10,11] or HfO_2. ALD silicon-nitride/SiO_2 stack gate dielectrics [12-15] are also a promising application for sub-100-nm technology nodes.

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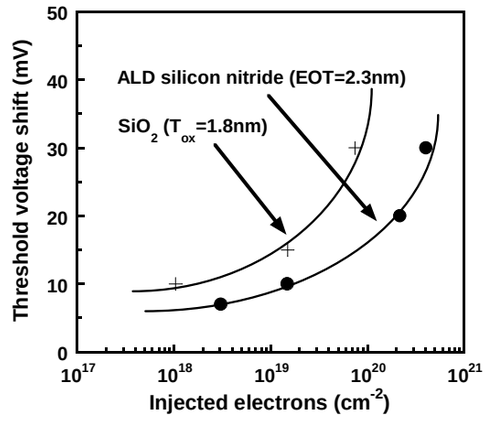

Fig. 1. Threshold voltage shift of ALD silicon-nitride and SiO_2 gate dielectrics after hot carrier injection. Hot electrons were injected by satisfying the forward bias condition between an n^+-injector (V_{inj} =-2.1V) and the substrate (V_{sub} =-1.2V) for the silicon-nitride sample. For the SiO_2 sample, V_{inj} =-3.2V and V_{sub} =-2.3V was applied. The same forward bias voltage (0.9V) was applied to the n^+-injector/substrate junction for both samples.