Effects of Low temperature NH_3 treatment on HfO_2/SiO_2 stack gate dielectrics fabricated by MOCVD system

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The effects of post-deposition low temperature (~ 400℃) NH_3 treatment (LTN) on the characteristics of HfO_2/SiO_2 gate stack with TiN gate electrode were studied in this work. HfO_2 films were deposited using AIXTRON Tricent® MOCVD system. Subsequently, the LTN treatment was implemented prior to post-deposition annealing (PDA) in order to avoid the growth of additional interfacial layer frequently seen as the high temperature nitridation technique is used. The effective electrical oxide thickness (EOT) for the samples without LTN was estimated to be 2.3 nm using CVC model [1] without considering Quantum effect. Figure 1(a) shows the high frequency (100kHz) capacitance-voltage characteristics of all samples subject to various PDA conditions. It was clearly observed that the distortion occurred in C-V curves can be significantly suppressed with higher PDA temperatures and LTN can help alleviate the distortion at lower temperature range. This hump is believed to be closely related to the presence of fast interface states since their positions are located between the flatband voltage and the threshold voltage. Moreover, the LTN treatment can effectively reduces the EOT, which is speculated to arise from the increase in K value of the gate stack. The frequency dispersion rate is displayed in Fig 1(b). For the samples without LTN, frequency dispersion rate becomes much worse upon increasing PDA temperature with respect to the samples with LTN.

SILC is an important concern in scaling gate oxide thickness because it can decrease DRAM refresh times, degrade EEPROM data retention, and degrade MOSFET off-state power dissipation. SILC is mainly cause by the trap assisted tunneling and then trap generation rate is an index of estimation for SILC [3]. Fig. 2 shows the comparisons of the trap generation rate of the samples under constant voltage stress (CVS) at V_g= -3.75V. The LTN can significantly reduces the trap generation rate compared to without LTN and, especially, the sample with higher temperature PDA (700℃) still exhibits extremely low trap generation rate, which means that LTN can dramatically improve the thermal stability of thin film.

Our experimental results indicate that the low temperature NH_3 treatment can not only effectively improve the characteristics of HfO_2/SiO_2 stack gate dielectrics, such as C-V characteristics, frequency dispersion and trap generation rate but also reduce the resultant EOT.

References

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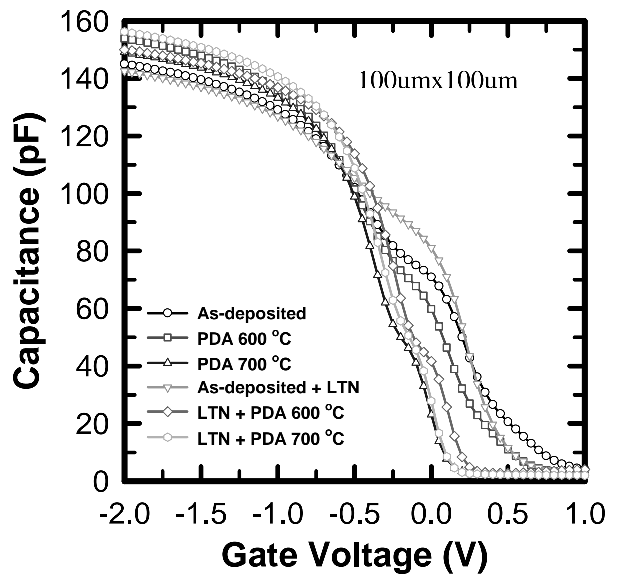
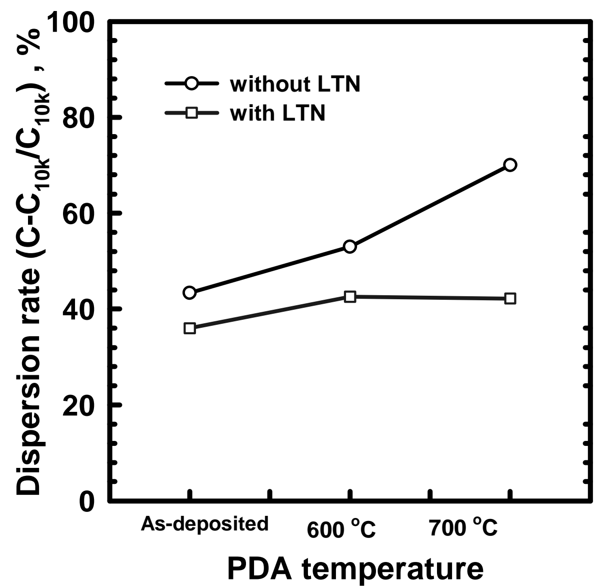


(a)



(b)

Fig 1 (a) The C-V characteristics (b) Frequency dispersion rate of HfO2/SiO2 gate stack for various PDA temperature treatments.

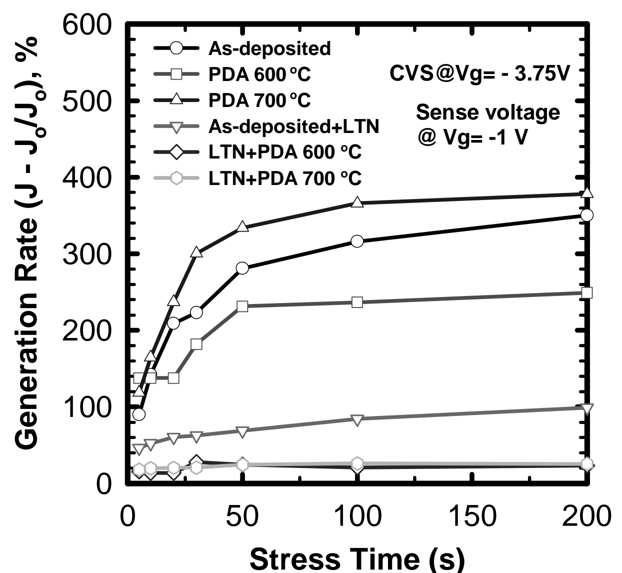


Fig. 2 Trap generation rate of HfO_2/SiO_2 gate stack under constant voltage stress (Vg=-3.75V).