Etching of Dual Doped Poly-Si Gate Employing Novel Microwave Plasma Generation with RLSA

T. Nishizuka[1], T. Nozawa[1], K. Ishibashi [1], T. Goto[2], T. Ohmi[2]
[1]KTC, Tokyo Electron LTD, 1-8 Fuso-cho, Amagasaki, Hyogo, 660-0891, Japan
[2]New Industry Creation Hatchery Center, Tohoku University, Sendai 980-8679, Japan

[Introduction]

The stable and uniform plasma etching system applicable to wide range process such as gate etching has been desired to get precise CD (critical dimension) control with high throughput. Microwave plasma shows potential of good etching performance; however, it has been difficult to get stable and uniform over various conditions. In this paper, newly developed plasma source and etching performance are demonstrated.

[Experiment]

Plasma was generated by microwave (2.45GHz) through RLSA (Radial Line Slot antenna) which consists of slot and dielectric plate (Fig.1)[1]. Process gas is supplied into chamber through shower head. Plasma density was measured by Langmuir probe system. Dual gate poly-Si etching was evaluated by this plasma source, and charging damage was also evaluated.

[Result and Discussion]

Figure 2 shows an example of plasma density distribution of several plasma conditions. Its profiles are flat and almost same independently of pressure or gas chemistry. The plasma can be generated in further low pressure below 0.1Pa. It was achieved by optimizing slot pattern, dielectric plate thickness and shape so that mode jump become reduced.

Figure 3 shows SEM photograph of the cross-sectional view of dual-doped poly-Si gate line and space pattern. This result was obtained under the condition of Ar/HBr gas. Etching rate ratio of N^+ /P^+ was 1.05 and CD ratio was of N^+ /P^+ is 1.02. Poly-Si etching followed resist trimming, hard mask etch and ashing which were also processed by same chamber.

Plasma charge up damage was evaluated with antenna MOS structure TEG in both etching and ashing conditions. Break down of SiO_2 dielectric (4nm) was not observed at all even on 1M antenna ratio.

[Conclusion]

Uniform plasma density distribution in wide process range was obtained by optimizing slot and dielectric plate. Charging damage free plasma etching and a good dual-doped poly-Si gate etching were demonstrated. Moreover it is expected that this system enables multi step etching in one chamber.

[1] T.Ohmi, Semiconductor manufacturing, p110, November 2003.

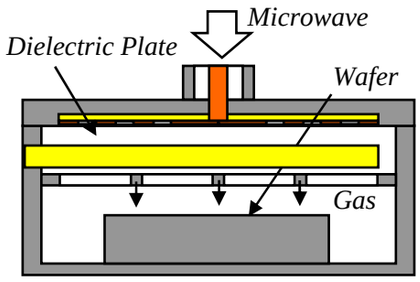

Figure1: Experimental apparatus

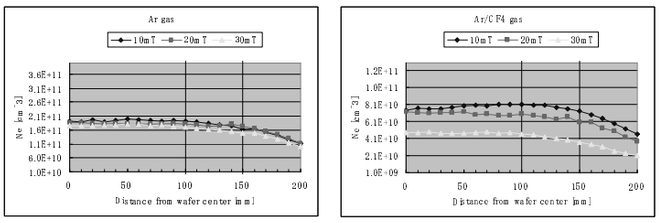

Figure2: Plasma density distribution in several conditions

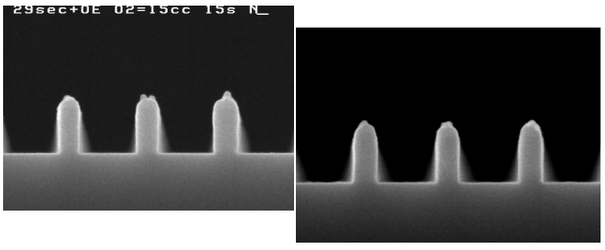

Figure3: Dual Poly-Si gate etching result