Scaling Trends and Advances in Metal Technologies for On-Chip Interconnects

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Scaling of feature size allows to increase the density of the devices and reduce the device cost. Intel launched the microprocessor using 90nm technology at the end of 2003. To continue scaling the following issues need to be addressed for on-chip interconnects including the increase of Cu line resistance due to larger relative volume occupied by the barrier layer and the increase of the impact of grain and surface scattering, complete gap fill with narrow openings (<30 nm) after barrier/seed deposition, the increase of Cu line EM resistance due to increase of current densities and introduction of Pb-free bump metallurgy. This paper will describe the advances of Intel's metals to address sub 90 nm scaling issues.

Barrier layer. Copper requires diffusion barrier due to rapid diffusion into Si and interlevel dielectrics (ILD). However, the barrier occupies larger space and increases the effective line resistance with decreasing the feature size. Thin barrier (about 1 nm) deposited by ALD can be used to mitigate the problem. Figure 1 show TEM cross-section of ALD TaN barrier with electroless Co cap. The reduction of the effective Cu line resistivity with ALD barrier can be more than 10% for sub-90 nm features. Adhesion of ALD barrier to dielectric, Cu adhesion to barrier layer, electromigration resistance and integration with low K ILD will be presented

Cu gap Fill. Plating transient effects become dominant for sub 90 nm features when the gap fill occurs during the first few seconds of the deposition. Since the adsorption rate of the accelerator is slower than that of the suppressor but the diffusion is faster, bottom up fill for this feature size becomes dominated by the effect of suppressor. In addition, PVD seed leaves <30 nm opening to fill, therefore direct plating on barriers will be needed. Figure 2 shows superfill of sub-micron features achieved by using direct electroplating on Ru barrier. Different technologies (ALD, CVD, PVD) will be discussed to deposit thin Ru barrier as well as characterization data for direct Cu plating on thin barrier will be presented including resistivity, roughness, adhesion etc.

Capping layer. Copper surface is dominant diffusion path causing failure during electromigration of Cu metallization. To improve adhesion of capping layer and therefore improve electromigration resistance, metal capping layer can be used. The use of electroless Co cap allows to increase EM MTF 10x+ with equivalent resistance to copper (Figure 3) as well as decrease Keff by about 10% if SiN(C) etch stop is eliminated. Since EL Co bath is intrinsically unstable, the special precaution needs to be taken to reduce defects (particles) and achieve 100% selectivity. The characterization of EL Co film properties such as adhesion to Cu and ILD, barrier and corrosion properties as well as microstructure will be presented.

Pb-Free bumps. PbSn bumps are being replaced by Pb-free bumps due to health and environmental concerns. Two possible materials are widely investigated as Pb-free bump materials such as Sn and Cu. Figure 4 shows the SEM view of smooth and uniform Sn bumps. The characterization of Pb-free bumps such as uniformity, adhesion, morphology, shear testing, reflowability, wettability etc will be discussed.

The novel metal process technologies and materials are being investigated for the introduction in sub-90 nm technology generations to reduce the effective Cu line resistance by using ultra-thin ALD barriers, increase Cu interconnect electromigration resistance and reduce the effective dielectric constant by using metal cap (EL Co) as well as implement Pb-free bumps.

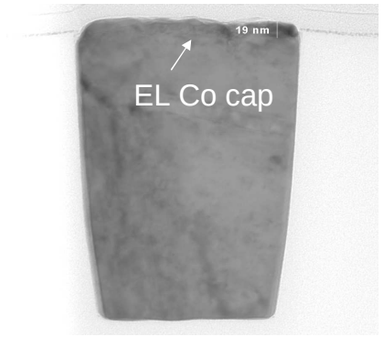

Figure 1. TEM cross-section of ALD TaN barrier and EL Co Cap layer

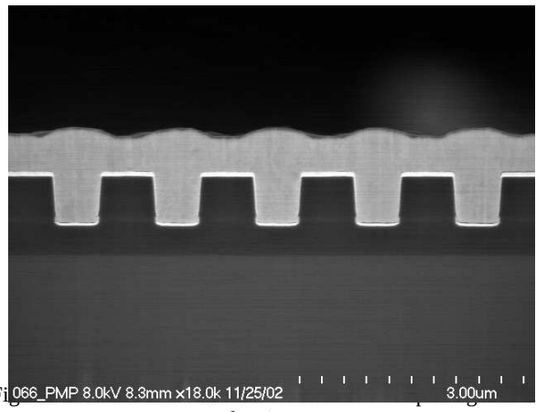

Figure 2. SEM cross-section of superfill of sub-micron features achieved by using direct electroplating on Ru barrier.

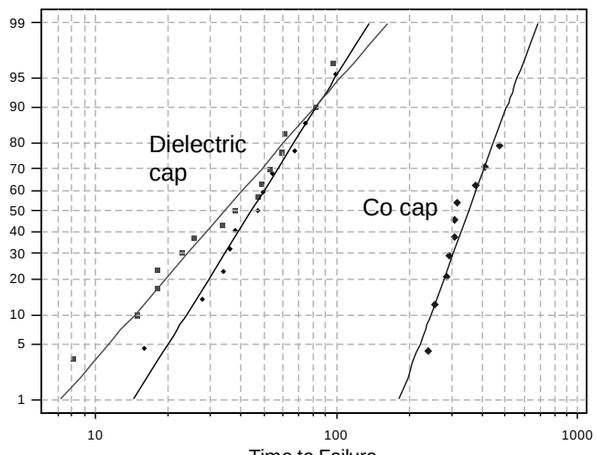

Figure 3. Electromigration lifetime improvement with electroless Co cap and metal capping layers

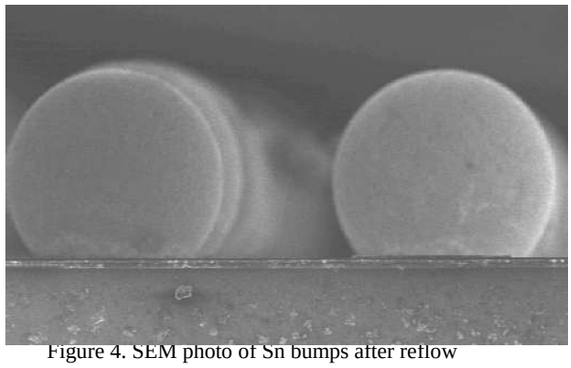

Figure 4. SEM photo of Sn bumps after reflow