Impact of Low k Dielectrics on Cu Interconnect and Packaging Reliability

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With device scaling continuing beyond the 90nm node, materials with a low dielectric constant (k) is being implemented to replace oxide in Cu interconnects. Compared with oxide, low k dielectrics are softer, expand more and conduct less heat. The weak thermomechanical properties significantly impact the reliability for Cu/low k interconnects and have stimulated great interests to study Cu/low k interconnect reliability. Recently, packaging assembly of Cu/low k chips has emerged to become an important reliability issue, particularly for plastic flip-chip packages. This paper discusses the reliability issues for Cu/low k interconnects, focusing on the impact due to the thermomechanical properties of low k dielectrics. Several basic questions arise concerning the dielectric effects on interconnect reliability including the rate of mass transport, thermal stress and deformation behavior and failure mechanisms. In this paper, we will address these issues and highlight some recent advances in understanding and improvement of EM and packaging reliability. We will first discuss how materials and processes of the damascene structure lead to distinct characteristics and mechanisms for EM and packaging reliability of Cu interconnects. Then the impact of low k dielectrics on packaging reliability will be examined using a multi-level sub-modeling approach to investigate interfacial delamination in Cu/low k chips. Results on packaging reliability will be discussed by comparing Cu/oxide and Cu/low k interconnects. Finally, we will discuss recent advances and approaches developed to address these reliability challenges.