Reliability of Cu Interconnects with CVD Low k BEOL Dielectric for 90nm CMOS Technology

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Copper metallization has been implemented for BEOL interconnects for its lower conductivity, which is required for sub-micron high performance products. The performance of interconnects can further be enhanced by integration of Copper with CVD low k dielectric.The 90 nm technology with Copper and low k allow 10 levels of wiring with and one level of Al Cu terminal level. In this technology first eight levels are made in low k insulator and the last two levels are made with FTEOS.All Copper levels except M1, are made with dual damascene Recent results obtained on electromigration, stress migration, time-dependent dielectric breakdown (TDDB) , thermal cycles and chip package interaction for Cu damascene structures in CVD low k will be discussed. The results of electromigration, thermal cycles, TDDB and stress migration stressing show that these results meets or exceed the requirements and equal those of Cu with oxide build.