A Novel Post Etch Cleaning Process to Prevent Titanium Corrosion in 90 nm Technology

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Negative Bias Temperature Instability (NBTI) has become one of the dominant reliability concenrns in deep sub-micron technologies. One of the methods to improve the NBTI lifetime is to use Ti-TiN bilayer Local Interconnect [1]. However, because the borderless or zero enclosure contact design rule is adopted for sub quarter micron technology, the surface of the underlying contacts connected to Ti-TiN metal lines will be exposed to the chemical solutions during wet clean after etch. This would lead to higher contact resistance from removal of Ti layer (anode in the electrochemical reaction) [2,3], and causes sort failure. This electrochemical corrosion reaction can be inhibited by replacing the EKC 265 with other type of solvent with PH of 5 [2], which is not easily accomplished in a well-established fab production environment due to adding cost and complication to the chemical distribution system.

This paper demonstrates a new post Ti/TiN etch cleaning process by plasma treatment followed by DI rinse without using solvent wet clean. The effectiveness of the new process was verified on the defect review and 72 M SRAM devices sort yield. Fig. 1 shows the schematics of cross-sectional view of Local Interconnect structure used in this study. Equivalent defect performance can be obtained with new post etch cleaning processes without using EKC 265 solvent clean. As shown in Fig. 2, no differense is obserbed in top down SEM images between Ti/TiN bilayer local interconnect using EKC solvent clean, and using plasma treatment plus DI rinse without EKC. No surface residue was observed on both treatments and the level of cleaness was also comparable. Fig. 3 showed the end of line sort yield results with different post etch cleans. The conventional clean using EKC 265 solvent showed unstable lower yield. The bit-directed failure analysis from Fig. 4 clearly indicated that Ti was attacked and created voids in TiN/Ti/W interface which was caused by the electrochemical Galvanic corrosions from hydroxyamine solvent at PH > 11. However, with the new proposed plasma treatment with DI rinse, the low sort yield can be recovered.

REFERENCE

1. Cypress Semiconductor, patent pending.
2. Leong-Tee Koh, et al, “Titanium Corrosion in 0.25um Metal Interconnects”, IITC p47, 1999.
3. Jang-Eun Lee, et al, “Plasma Charge-Induced Corrosion of Tungsten-Plug Vias in CMOS Devices”, IITC p273, 1999.

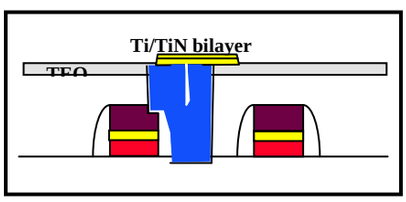
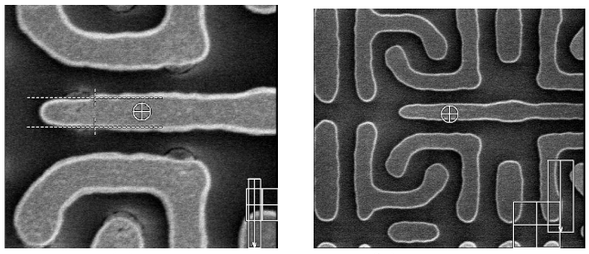


Fig. 1. Schematics of cross-sectional view of Local interconnect structure.



(a) (b)

Fig. 2. Top down SEM review showing clean surface (a) with EKC clean, and (b) plasma treatment with DI rinse without EKC.

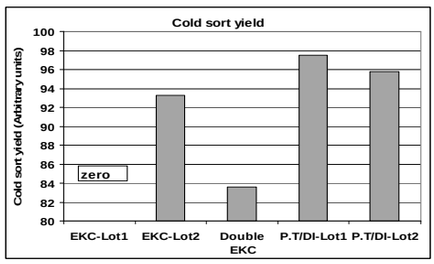
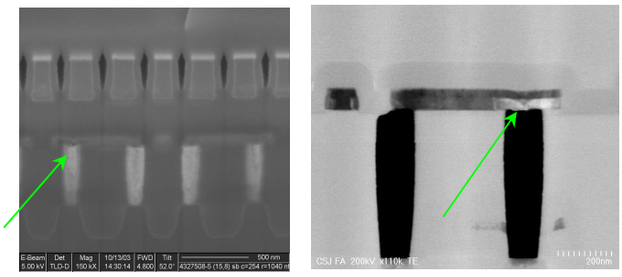


Fig. 3. Cold sort yield comparison between EKC clean, double EKC clean, and plasma treatment + DI rinse (P.T/DI) without EKC



(a) (b)

Fig. 4. SEM(a) and TEM (b) showing Local Interconnect with Ti corrosion, by bit-directed Failure Analysis.