Tungsten Hard Mask Damascene Integration Scheme for 65nm

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Abstract

Smaller geometries and the use of lower κ dielectrics in BEOL integration at 65nm and beyond will require extensive changes in dual damascene (DD) integration scheme. This paper presents the development of a tungsten hard mask (HM) integration solution for extending the implementation of copper/low-κ interconnect structures. The scheme overcomes major challenges in low-κ integration, minimizing ashing damage to low-κ material and avoiding photoresist poisoning issues associated with 193nm resist. From the perspective of feasibility and cost, tungsten HM integration appears to be a promising candidate for DD integration

Introduction

The semiconductor industry has been constantly pressured to deliver faster devices while lowering fabrication costs. As critical dimensions decrease, circuit performance is limited by the interconnect signal resistance and capacitance (RC) delay that led to the adoption of copper/low-κ interconnect structures.

The transition from the 130nm technology node to the 90nm and especially the 65nm node imposes two important changes in the materials used for interconnect integration. First, mature DUV resist (248nm lithography) is being replaced by 193nm resist that is softer and more susceptible to "poisoning." Second, FSG is being replaced by low-κ carbon doped silicon dioxide (SiOC with k<3.0 and k<2.6) that are mechanically softer (lower modulus) and more susceptible to damage during ashing [1].

Different approaches have been proposed and used to minimize resist poisoning. Full organic BARC/PR via fill, a direct extension of the partial BARC fill approach, requires strict control of the low-κ etch to minimize fencing and faceting of the via corners [2]. Using Sacrificial Light Absorbing Material (SLAM) [3] minimizes fencing and faceting during the low-κ etch but its removal requires a wet clean that may damage the low-κ film. .

Here we propose using a trench-first HM approach that minimizes low-κ damage during ashing.

HM Dual Inlaid Interconnect

Figure 1 shows a typical patterning of a dual damascene structure using the HM approach. After interlayer dielectric (ILD) and HM deposition, the trench HM is first patterned and etched. Planar BARC fill is then deposited to facilitate via lithography without poisoning. Thereafter, via is partially etched, the resist stripped, and the HM trench exposed. The trench is then etched while via is being etched to the bottom. Finally, the bottom barrier is removed. Note that if low-κ material is damaged during the partial via etch/Ash, it will be mostly etched away during trench etch, thus minimizing low-κ surface modification.

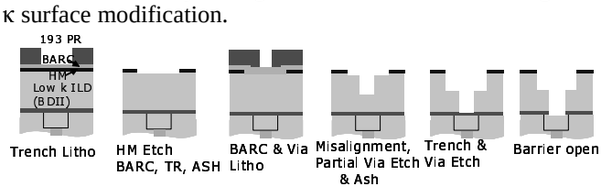

Fig 1. Interconnect damascene patterning using a HM approach. Most of the low-κ ILD damaged during via ash will be removed during the trench etch. Before via partial etch, a misalignment correction step must be used to open a portion of the via covered by the HM as a result of lithographic misalignment. The number of steps is the same as a typical full-BARC-fill via-first approach. The etch-back step is replaced by HM deposition.

HM Feasibility Study

The feasibility of using a HM was investigated on 300mm wafers. Next-generation ILD (κ ~2.7) and barrier materials were deposited using the Producer™ platform. HM materials were deposited using PVD Endura™. Metal etch was performed by the DPS™ II and all-in-one dielectric etch was performed by the Enabler™[2]. CMP feasibility was investigated using a Mirra Mesa™ platform.

We explored the use of titanium nitride (TiN), tungsten (W), and amorphous silicon as potential HM materials. The latter failed to meet selectivity requirements for mask open and trench etch. TiN showed good selectivity during mask open and trench etch, but unless a specific treatment was applied to the mask, residue was observed following the trench etch. However, tungsten HM behavior was similar to that of soft masks; therefore similar chemistries could be used during trench etch and the mask maintained integrity superior to that of the TiN.

All-in-One Via and Trench Patterning

Tests were conducted using ILD materials with κ values of approximately 2.7 and 3.2. ILD patterning was conducted using the Enabler Clean Mode™ reactor. The first step was to selectively remove BARC, stopping on the low-κ layer to minimize effects of BARC non-uniformity. After this, the via was partially etched, followed by a dry ash to expose the trench HM. Trench and via are finally etched (Figure 2).

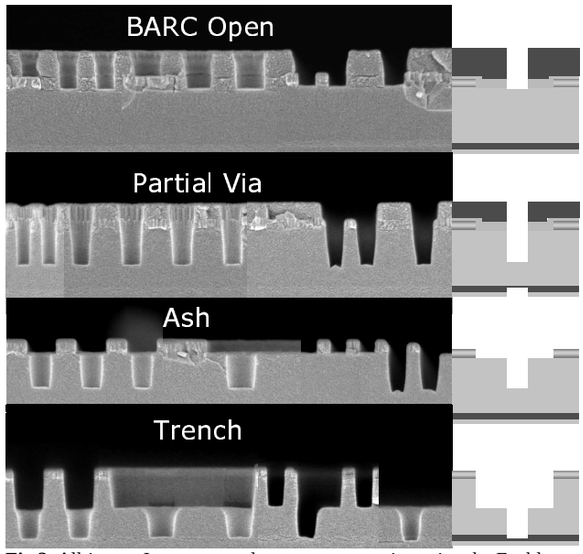

Fig 2. All-in-one Interconnect damascene patterning using the Enabler reactor.

Summary

This abstract addressed the feasibility of HM scheme using tungsten for extending the implementation of copper/low-κ interconnect structures. The proposed interconnect patterning technique requires the same number of process steps as conventional via-first patterning, avoids 193nm resist poisoning, and minimizes low-κ ILD ashing damage. The feasibility of the approach was demonstrated by good results achieved on porous SiCO (k~2.7) ILD. The trench patterning process with a tungsten HM used chemistries similar to those for soft mask patterning. The tungsten HM maintains good integrity after etching. Moreover, low-shear force CMP also demonstrated good W removal rates. From the perspective of feasibility and cost, tungsten HM integration shows considerable promise.

References

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