**HOT-CARRIER INSTABILYTY IN N- AND P-CHANNEL POLY-Si TFTS**

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Hot-carrier degradation in n- and p-channel low-temperature poly-Si TFTs under systematic DC stress bias condition is studied.

Laser annealed poly-Si film thickness was 50nm and plasma-CVD gate oxide was 140nm thick. N- regions for n-channel LDD TFTs and heavily doped $p^+$ source and drain regions for p-channel TFTs were self-aligned to the metal gate electrode. W/L mainly used were 9 $\mu$ m and 4.5 $\mu$ m, respectively. Substrate and gate current were measured and hot-carrier stress was applied for both type devices.

Fig.1 shows the threshold voltage change ($\Delta$ Vt) after each stress gate voltage (Vsg) for n-channel LDD TFTs for stress times of 100, 1000, and 10,000sec at a fixed stress drain voltage (Vsd) of 12V. Vt is defined as the gate voltage for drain current of 0.2 $\mu$ A/ $\mu$ m of channel width at Vd=0.1V. Under strong current saturation stress, Vt changes to negative direction and to tend to saturate with the increase of stress time, and the degradation is worst at the gate voltage corresponding to the largest substrate hole current as is reported in bulk-Si n-channel MOSFETs[1]. $\Delta$ Vt and $\Delta$Gmmax in short stress time has exhibited a power-time dependence of the form $At^n$ [1],[2] with an exponent n=0.5, which could be due to the interface state generation at poly-Si/gate oxide interface and in the grain boundaries in poly-Si[3]. Saturation of the degradation is supposed to be due to the combination of an increase in barrier height and a decrease of conduction near the drain owing to the state generation near the drain. Under weak current saturation stress, $\Delta$ Vt shows to increase with the stress time in longer stress time showing the n=0.4. Under the deep gate and drain bias, electrons and holes could be injected into the gate oxide, and the degradation could be due to the interface state generation at the interface and grain boundaries.

Fig.2 shows the $\Delta$ Vt after each stress gate voltage for p-channel TFTs at Vsd=–12V. Under strong current saturation stress, Vt changes to positive direction and its shift shows maximum at Vsg=-2V corresponding to the threshold voltage showing the largest electron gate current [4]. $\Delta$ Vt tends to saturate in the case of longer stress time. The exponent n takes values of around n=0.1 in the shorter stage of stress time, which is due to the trapping of hot-carrier-induced hot-electron near the drain giving rise to shortening of the effective channel length [5]. The $\Delta$ Vt saturation would be due to the decrease of the lateral field near the drain owing to trapped electrons, which is supposed by the observed decrease of kink current and substrate current after stress. Under the weak current saturation stress, Vt shifts to negative direction corresponding to the observed gate hole current, and continues to increase with increasing stress time, especially for deeper Vsg such as –12 to –14V and the n-values around n=0.3 or more. This result for deeper Vsg suggests that hot holes are trapped and also the interface states with positive charges (donor-type interface states) are generated at the interface and grain boundaries in poly-Si. In longer time the degradation in weak current saturation stress could be worse than that in strong current saturation stress.

**References**

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Fig.1 Vt shifts against stress gate voltage

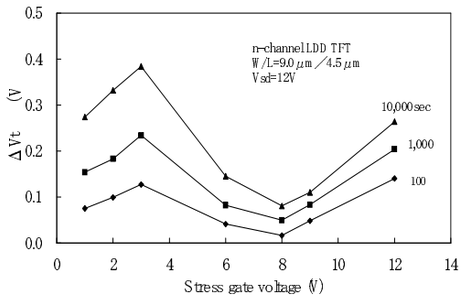


Fig.2 Vt shifts against stress gate voltage