Modelling of Source Gated Transistors in Amorphous Silicon

F. Balon and J. M. Shannon
Advanced Technology Institute, SEPS, University of Surrey, Guildford, GU2 7XH, UK

A new form of thin film transistors (TFT) was introduced recently named the Source Gated Transistor (SGT)[1]. The basic principle of operation is different from a conventional field effect transistor (FET) where the electrical field induced by the gate modulates the channel conductance and current saturates when the semiconductor region at the drain end is depleted.

In the SGT the electric field induced by a gate located directly below the source is used to change the effective barrier height (i.e. magnitude of the current) and current saturates when the semiconductor underneath the source barrier is depleted of carriers by the reverse biased barrier. Fig.1 shows a schematic drawing of the SGT transistor.

The SGT has many advantages over a conventional FET such as excellent output characteristics with low saturation voltage and very high output impedance. An example is shown in Fig.2. Moreover the SGT shows good device stability at low currents, which allows us to consider these devices for analog circuits. Short channel effects are also reduced in the SGT.

The source barrier is a vital part of the SGT concept. Therefore a full understanding of the behavior of the source barrier is necessary in order to characterize these devices. Here we are reporting on the source modeling of the SGT in a-Si:H, in particular how the barrier height and area of the source influence device performance. These issues are related to the validity of the dielectric model [2] and stability of the SGT. All simulations were done with the developer version of the ATLAS Silvaco (v.5.7.28.C) with the latest implementation of the model for the barrier tunneling and lowering mechanism.

For an FET biased into the on-state the electron quasi-Fermi level moves towards the conduction band in the channel region. This is consequently accompanied by a rise in the electron concentration (Fig.3) and there is an increase in the generation of defect states (i.e. silicon dangling bonds) that trap electrons and cause a voltage shift and current instability of the FET. However in the SGT the region underneath the source barrier is depleted after current saturation so the quasi-Fermi level is close to the thermal equilibrium state. Therefore fewer states are generated in the a-Si:H and the device is much more stable.

The saturation voltage (V_{SAT}) in the SGT is very well described by a dielectric model which shows that the change in V_{SAT} per one volt change in gate voltage (V_{GS}) can be 10 times lower than in an FET. However when the barrier height Φ_B is decreased from 0.5eVdown to 0.3eV the saturation voltage is shifted towards higher values. This is due to higher amount of electrons crossing the reverse biased barrier and lack of well defined depletion.

The current (I_D) through the SGT is determined by a reverse biased source barrier i.e. it mainly depends on the Φ_B, tunneling constant and area of the source. It has been shown that I_D scales linearly with the source width but is independent of source-drain separation *d* [3].

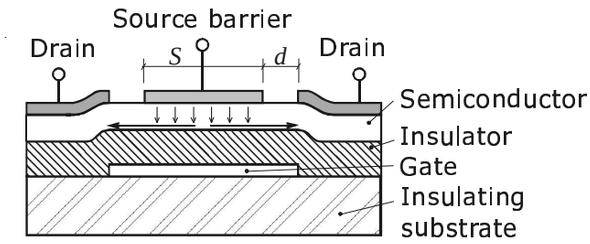

Fig.1. Shows schematic drawing of SGT transistor. The gap between source and drain is defined as the source-drain separation.

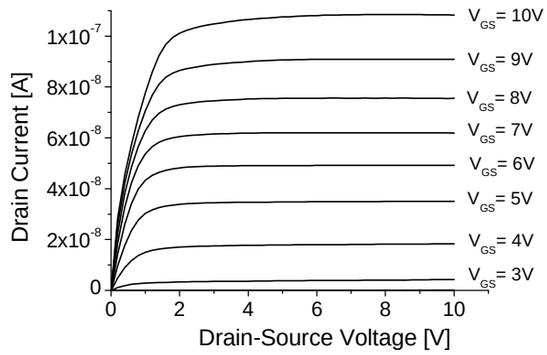

Fig.2. Shows experimental SGT transistor characteristics. The width of the device and source-drain separation is 12um and 2um respectively.

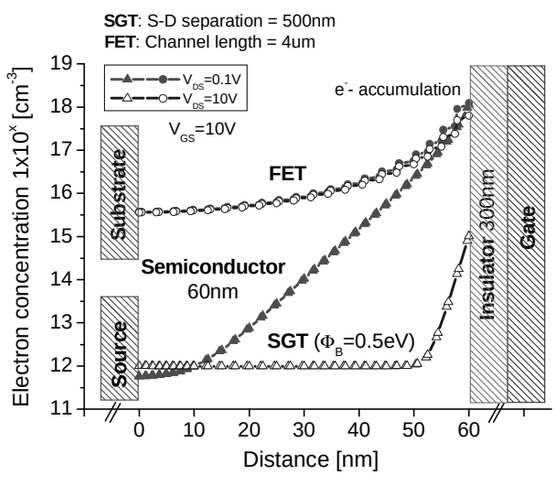

Fig.3. Shows simulations of the electron concentration (i) underneath source barrier (Φ_B=0.5eV) of SGT and (ii) 100nm from the source region of an FET.

In case of source length *S* the I_D increases linearly with *S* for high Φ_B however for lower Φ_B has a tendency to saturate with increasing source length *S*.

A comparison between simulated and experimental results show good qualitative agreement, and allows us to predict the behavior of SGT devices before their fabrication.

References

[1] J. M. Shannon and E. G. Gerstner, IEEE Electron Device Lett. **24,** 405 (2003)
[2] J. M. Shannon and E. G. Gerstner, Solid State Electronics **48,** 1155 (2004)
[3] J. M. Shannon and F. Balon submitted to ESSDERC 2004 conference.