Thin Film Transistor Models for Circuit Simulation
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Modeling of Thin Film Transistors (TFTs) presents unique challenges related to a rich variety of observed TFT characteristics and many non-ideal features affecting their performance. These non-ideal characteristics are related to the gate voltage dependent field effect mobility, distributive nature of gate-to-channel capacitance, gate voltage dependent series source and drain resistances, non-ohmic contacts, gate and drain bias voltage stress effects, and short channel effects that are very pronounced even in relatively long channel devices. Localized states play an important role in all TFTs as illustrated in Fig. 1 that compares the distributions of localized states in a-Si and poly-Si with the absence of such states in crystalline silicon. Amorphous silicon and polysilicon TFT models are better established than models for nanocrystalline silicon (nc-Si) TFTs and Organic TFTs (OTFTs). The unique properties of nc-Si have been reported very recently; see, for example, Fig. 2. OTFT characteristics strongly depend on the organic compound used and on the device design; for example, on the location of the source and drain contacts in so-called top contact and bottom contact TFTs (see Fig. 3). This paper will review physics-based TFT models suitable for implementation in circuit simulators, such as SPICE, with emphasis on modeling non-ideal effects, including modeling stress effects and non-linear gate voltage dependent series resistances. Comparison with measured data shows that these models adequately reproduce experimental data and are suitable for simulation of electronic circuits containing TFTs. We will also discuss low frequency noise in TFTs and link the device physics to the observed noise behavior. The low frequency noise in TFTs is primarily 1/f noise (see, for example, Fig. 3) and is several orders of magnitude higher than in their crystalline counterparts.

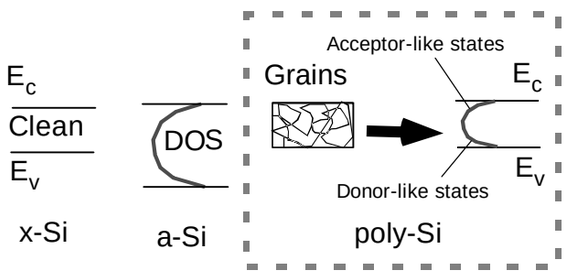

Figure 1. Energy band diagrams for crystalline silicon, amorphous silicon, and poly-Si. [1]

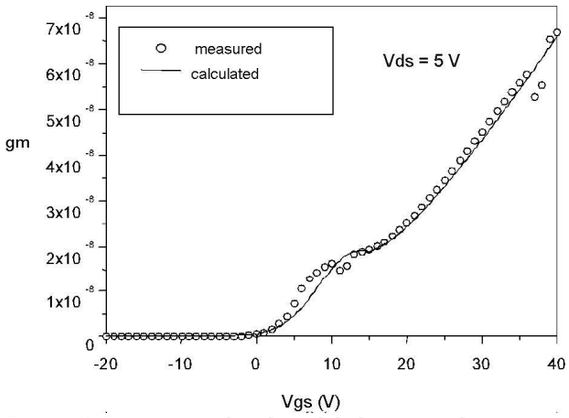

Figure 2. Experimental and modeled transconductance using the new nc-Si:H model.[2] © 2002 IEEE

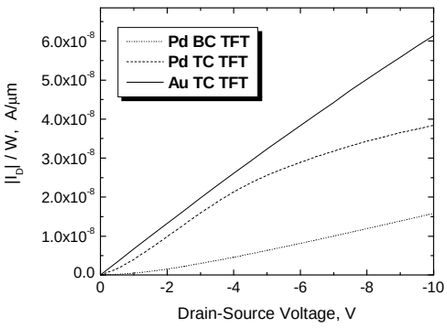

Figure 3. Top contact and bottom contact pentacene TFT (gate length) output characteristics (V_{GS} =-60V).[3]

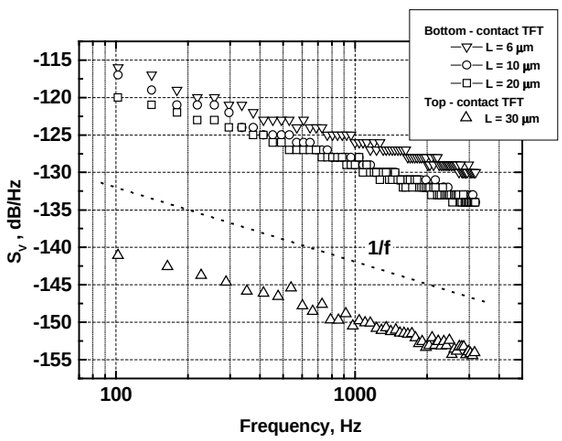

Figure 4. Typical spectral density of the voltage fluctuations S_V versus frequency for pentacene TFTs. 1/f line is shown for reference. [4]

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[1] B. Iñíguez, T. Ytterdal, T. A. Fjeldly, and M. S. Shur, Chapter 3, Physics and Modeling of Poly, Micro, and Nano Crystalline TFTs, in Poly-Si Thin Film Transistor, Volume 2, Edited by Yue Kuo, Kluwer Publishers Co. pp. 95-141 (2003)

[2] D. Dosev, T. Ytterdal, J. Pallarès, L. F. Marsal and B. Iñíguez, "DC SPICE Model for Nanocrystalline and Microcrystalline Silicon Thin Film Transistors," *IEEE Transactions on Electron Devices*, **49**, 1979 -84 (2002)

[3] P. V. Necliudov, M. S. Shur, D. J. Gundlach, T. N. Jackson, Contact resistance in pentacene thin film transistor, Solid State Electronics, Vol. 47, pp. 259-262 (2003)

[4] P. V. Necliudov, S. L. Rumyantsev, M. S. Shur, D. J. Gundlach, T. N. Jackson, 1/f Noise in Pentacene Organic Thin film Transistors, J. Appl. Phys. Vol. 88, No. 9, pp. 5395-5399 (2000)