System Displays and TFT Process and Device

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1. Introduction

The system display is an innovative concept for next-generation displays in which informationprocessing functions are integrated on a glass together with pixel arrays. Signal processing capabilities, such as decoding and DA conversion, have already been integrated on panels, and this has resulted in highresolution, area-efficient displays. These displays are widely used in color cellular phones and PDAs. Even higher levels of integration are expected in the next several years (Fig. 1).

2. System Display Application

System displays will have an enormously wide range of applications. For example, they could be the basis for ultra-thin card-type viewers combining wireless communications, image processing, biometric identification, and a ultra high-resolution screen. These viewers might be replacements for credit cards in use today. Moreover they could be used in Mobile Net TVs that will seamlessly extend image-based entertainment into the realms of communications and computations. **3. System Design and Cell Library**

A wide variety of system functions will be needed for any application. Consequently, the functions to be integrated on the panel will have to be designed systematically by using a higher-level system description language. For this purpose, a library of MACRO cells, such as NOR, NAND, D-Flip-Flop, SRAM etc., has to be developed (Fig.2). Cells are described as a set of information, including logical behavior, speed, dissipation power, mask layout, and process condition.

4. TFT and Key Process

TFTs fabricated on a glass substrate are key devices for system displays. TFTs with submicron feature sizes and large mobilities of around 500 cm²/Vsec are fast and sufficiently have high drivability at clock frequencies higher than 100 MHz. Technological advancements in materials science and technology integration will lead to the realization of high performance TFTs.

Crystallization

TFTs are fabricated with a crystallized Si layer on the glass. The size of the crystallized area has to be large enough to accommodate several submicron CMOS devices in it. To form large crystallized areas at any predetermined position, phase modulated excimer laser annealing (PMELA) is supposed to be the only possible technology (Fig.3). The details of the technology will be given in another presentation at the conference.

Gate Insulator

Achieving a TFT gate length in the submicron range will require a gate insulator layer as thin as 30 nm and a low interface state density. Microwave plasma enhanced CVD makes it possible to form a high-quality insulator, while keeping the maximum process temperature less than 500°C.

4. Conclusion

The technology direction toward system displays on the basis of state-of-the-art TFT process is discussed. The importance of standard cells as building blocks of an integrated system on panel is emphasized.

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Position-controlled large grains were grown by using cross-coupled modulators.

Fig.3 Phase Modulated Excimer Laser Annealing