HIGHY MOBILITY TOP-GATE MICRO-CRYSTALLINE SILICON TFTs PROCESSED AT LOW TEMPERATURE (<200°C)

A. Saboundji, N. Coulon, C. Simon, T. Mohammed-Brahim, O. Bonnaud
GM-IETR, Universite RENNES I,
Bat.11B, Campus de Beaulieu, F-35042 Rennes Cedex,
FRANCE, brahim@univ-rennes1.fr

Now, the electronic devices, used to process the signal given by mechanical, chemical or biological functions, have to be made on the same substrate used for these other functions. In many cases, the substrate is a glass or a plastic that does not support high temperature. So, the electronic devices have to be processed at the lowest temperature that can be lower than 200°C. The basic electronic device is the field effect transistor that includes silicon active layer and source and drain regions as well as high quality gate insulator.

Silicon films can be deposited in the amorphous or crystallized state by PECVD at low temperature. Microcrystalline silicon is however more stable and can lead to higher electrical performances. High quality gate insulator deposited at temperature lower than 200°C is a more hard challenge.

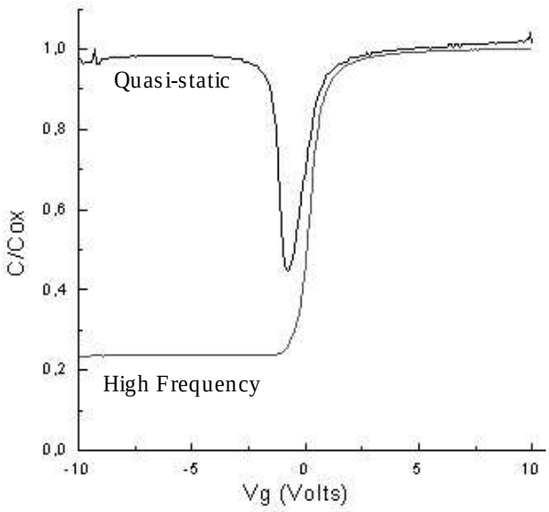
Here, silicon dioxide films were deposited by RF sputtering and then submitted to a plasma post-treatment without heating the substrate holder. Capacitance measurements of single crystalline silicon wafer / RF sputtered SiO_2 / Aluminium structures show a low Flat-Band voltage (~-0.2V) and an interface state density of ~4 x 10^{11} cm^{-2}.

N-type top gate Thin Film Transistors (TFTs) were fabricated using the previous silicon dioxide as gate insulator and microcrystalline silicon films as active layer. The highest temperature, 200°C, during the process is reached during the final forming-gas annealing of the aluminium contacts.

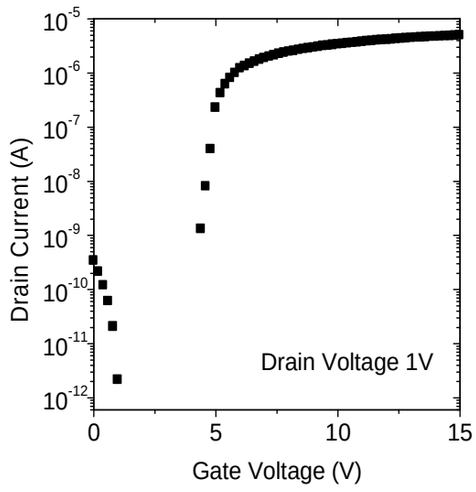
For the microcrystalline silicon, 400 nm thick single layer is deposited on glass, i.e. the undoped and doped layers are stacked during the same growth process, without breaking the vacuum and just by switching on the phosphine opening valve when the thickness of the undoped layer is assumed to be 200 nm. The doped layer is then plasma etched to define the source and drain regions. Finally the silicon dioxide gate insulator film, 115 nm thick, and the Aluminium contacts are deposited and then etched.

Microcrystalline TFTs resulted in a mobility of 40 $cm^2/V{\cdot}s$ and an inverse sub-threshold slope of 0.4 V/dec. The high mobility gives more chance to these µc-Si:H TFTs, fabricated using the present low temperature process, in the active addressing of OLEDs flat panels.

FTs.



Capacitance-Bias Characteristics of MOS structure using sputtered silicon dioxide film.



Tranfer Characteristics of Microcrystalline Silicon Top-gate T