Ultra low-temperature polysilicon TFTs on plastic substrate

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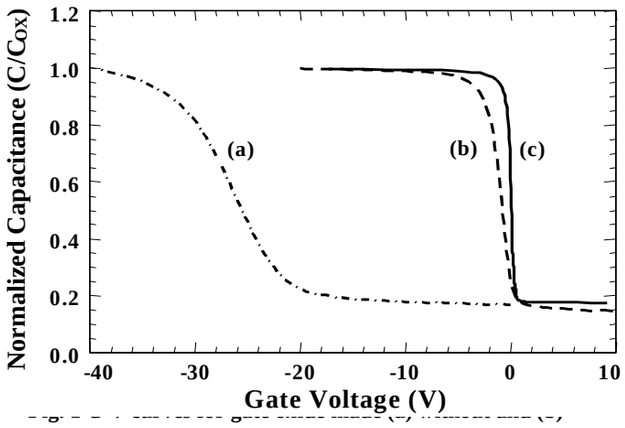
This paper describes an innovative ultra-low temperature poly-silicon TFT process fabricated on plastic substrates. Key technologies including room-temperature silicon and oxide deposition steps, laser crystallization, and transient dopant activation will be presented. Manufacturing problems related to plastic material compatibility in a TFT process are discussed and solutions are sought. An active matrix TFT backplane is fabricated with an OLED (Organic Light Emitting Diode) display to demonstrate this technology.

In this work, first, a novel plasma enhanced CVD system based on electron cyclotron resonance is developed to generate high density plasma near room temperature and deposit silicon dioxide films of excellent property. This process involves a pre-deposition step to oxidize silicon in (H_2+O_2) plasmas environment. It grows a very thin, but high quality oxide resulting in low Si-SiO_2 interface states. The C-V curves shown in Fig. 1 illustrate that the quality of the gate oxide obtained with a pre-deposition oxidation step approaches the theoretical limit calculated with no interface states. Second, a Xe-Cl excimer laser annealing system is made to crystallize sputtered silicon on plastic, thereby forming large polysilicon grains for TFT's with much higher mobility than its amorphous counterpart. The extremely short laser pulses provide sufficient energy to melt the deposited Si, while preserving the structural quality of the underlying plastic material. This laser system is successfully employed to fully activate impurity dopants and anneal damages introduced by ion implantation needed for source/drain formation..

To use standard automated semiconductor manufacturing tools, we has developed a lamination/de-lamination process to handle the flexible substrates. Both sides of the plastic wafer are coated with a hard-coat material that increases resistance to scratches and chemicals, and planarizes the plastic surface. The plastic wafers are then processed through a heat-stabilization cycle. This cycle relieves internal stresses and reduces plastic deformation in subsequent lithographic steps. Fig. 2 shows the run-out measured as dimensional changes at different radial locations of the 6-inch wafers between two successive photolithography steps. Using the heat stabilization treatment, the run-out is greatly reduced. In addition, the lamination process cannot trap air bubbles and needs to withstand wet processing and to be clean and dry to meet deposition chamber requirements such as minimum out-gassing. The laminated plastic needs to be delaminated safely from the glass carrier wafers after the TFT manufacturing process is completed.

To make a TFT integrated circuit, all process steps must be integrated. There are integration issues unique to plastic. For example, plastic is sensitive to stress caused by metal lines, we had to develop an Al/Mo composite metallization scheme for it. The compatibility of transparent metal, ITO (Indium Tin Oxide) in this case, to plastic substrate is another integration issue. Avoiding heat dissipation in plastic substrate during laser processing is yet another key consideration. Proper design of heat absorbing layer is needed. During source/drain implant activation, Si islands have already been formed, laser damage can occur in the area where the plastic substrate is no longer covered by a blanket silicon layer. To resolve this issue, we've embedded a Bragger reflector layer in between the plastic substrate and the Si layer. By using alternating oxide/nitride layers, plastic damage can be avoid.

A typical finished TFT device is shown in Fig. 3. After the plastic sheet is de-laminated, low off current is achieved using a 300˚C hydrogen plasma anneal process. Relevant device parameters are shown at the bottom of the figure. The ultra low-temperature polysilicon TFT process has been used to fabricate active matrix backplanes on glass and plastic substrates. The backplanes are used to make display demos with OLED. The image of the demos will be presented.



with pre-deposition plasma oxidation; (c) theoretical calculation with no interface states

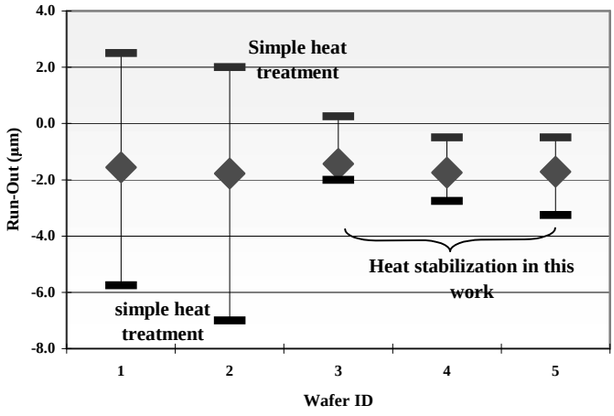


Fig. 2 Dimensional instability (run-out) in plastic and its reduction by heat stabilization

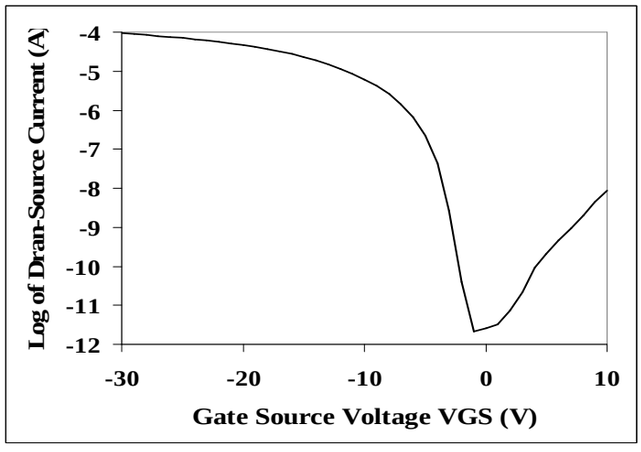


Fig. 3. I-V curve for a 4/20 *W*/*L* p-channel TFT fabricated on plastic substrate.

TFT Parameter	Median	Sigma
Hole mobility (cm^2/Vs)	71	9
Threshold voltage (V)	-4.8	0.25
Sub-threshold slope (V/dec)	0.59	0.09
Off current (pA)	2.7	1.2