Hydrogenated amorphous silicon bipolar thin-film junction transistors (a-Si:H B-TFTs)

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Compared with the field effect transistor (FET), the single crystalline silicon-based bipolar junction transistor has a large current driving ability and a high switching speed. However, the bipolar transistor has a large power consumption. The conventional a-Si:H TFT can be fabricated on a large substrate using low temperature PECVD films. However, the a-Si:H TFT suffers from a low on current and a slow switching speed due to high defect densities in the bulk a-Si:H film and at the a-Si:H/gate dielecric interface. If bipolar transistors can be fabricated using the low temperature plasma enhanced chemical vapor deposition (PECVD) a-Si:H films, limits on driving current and speed could be greatly reduced. In addition, since the a-Si:H film can be prepared as very thin, the power consumption can be low. In addition, since the a-Si:H film is amorphous, it will not form pipes between the emitter and the collector, which is a yieldkilling factor for the epi-based bipolar. Although there was a report on the B-TFT [1], the detailed device characteristics and fabricated processes were not studied.

In this study, we fabricated n-p-n bipolar junction transistors from a-Si:H thin films. As shown in Fig. 1, a stacked structure of $n^+/i/p/i/n^+$ of a-Si:H thin films was used to form emitter/base/collector layers. All a-Si:H layers were deposited by PECVD (Applied Materials Mark I) at 250°C. The passivation SiN_x was deposited using the same PECVD system. Totally, five masks, (i.e., for island, emitter via, emitter electrode, base island, and base electrode), were used to fabricate complete B-TFTs. Films were etched with reactive ion etching (RIE) (PlasmaTherm 700) or wet etching. The proper film thicknesses for good junction behaviors were obtained from the study of a-Si:H p-i-n junctions that were independently made.

Figure 2 shows the top view of a finished a-Si:H B-TFT. Figure 3 shows the common-emitter output characteristics of the B-TFT. A current gain of 3~6 was achieved, which is larger than the literature value [1]. The observed current noise might be attributed to the high defect densities of junction interfaces, especially the interface between base and emitter.

The "OFF" current of a few micro-amps observed in Fig. 3 leads to a rather low ON-OFF current ratio. This is attributed to the parasitic p-n diodes formed between the base and collector outside of the emitter active region. The high series resistance of the base layer is a major factor to the effect of parasitic diodes. Therefore, a large on-off current ratio is expected if the player thickness is increased or the i-layer thickness is decreased. However, the output characteristics are affected by the thickness change. An optimized thickness for each layer is critical to the best device characteristics.

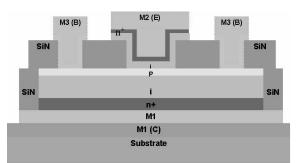


Fig. 1. Cross-sectional view of an a-Si:H B-TFT.

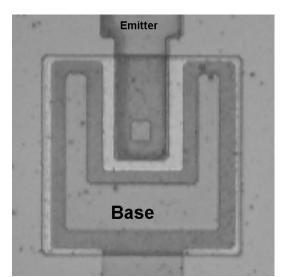


Fig. 2. Top view of an actual B-TFT device.

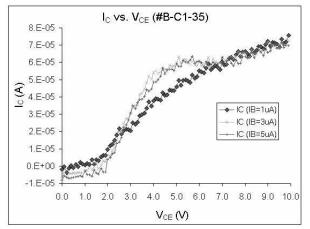


Fig. 3. The common-emitter output characteristics (I_C vs. V_{CE}) of an a-Si:H B-TFT device.

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[1] Y. Nara and M. Matsumura, *Japanese Journal of Applied Physics*, **23**(9), L714(1984).