New Pixel Circuit to Recover Vth Shift in a-Si TFT for Active Matrix OLEDs

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Introduction

The OLED technology has been increasingly attracted due to high efficiency [1]. Active matrix (AM) OLED employing poly silicon (poly-Si) or amorphous silicon (a-Si) thin film transistor (TFT) has problems to solve. Widely employed poly-Si TFT suffers from the inherent random grain size which causes non–uniformity. The a-Si TFT could be fabricated with low cost and reproducible characteristics. However, a-Si TFT exhibits a bias induced meta-stability phenomena that cause threshold voltage shift. Since the luminance of OLED is dependent on an inject current Id, which is proportional to $(Vdata-Voled-Vth)^2$, the increase of threshold voltage would induce inferiorities of OLED display. [2].

The purpose of our paper is to report the pixel circuit, which employs a negative bias annealing for a-Si:H TFT. It can recover the characteristics of degraded TFT and is verified by SPICE simulation.

Experiments and Design

The a-Si:H TFTs used in the experiments were the conventional inverted staggered structure. Fig. 1 shows bias waveform and transfer characteristics of TFT. The transfer characteristics were measured before and after gate bias stress. The threshold voltage of a-Si TFT is shifted to the positive direction. This instability was explained in two well-known mechanisms such as charge trapping and creation of defect state [3][4][5].

In case of the proposed polarity balance biasing, the threshold voltage shift is considerably suppressed as shown in Fig. 2.

Fig. 3 shows the pixel circuit and sequence employing polarity balanced driving scheme. The proposed pixel consists of two driving TFT with storage capacitors, switching TFTs, dual scan lines and analog inverters. The analog inverters supply negative bias adjacent driving TFT in order to recover the a-Si:H TFT.

When the scan m ($2N-1^{th}$ frame) is high, SW1/3/6 turn on. The data signal is stored at the storage capacitor (Cst1) to maintain the data during one frame so Dtr1 provides the current for the OLED. At the same time, the data signal enables the Inv2 block to turn on. Thus, adjacent driving TFT (Dtr2) is annealed by negative bias, which is supplied from analog inverter (Inv2 block). Conversely, when scan m' ($2N^{th}$ frame) is high, the pixel circuit operates in the same process at the $2N-1^{th}$ frame.

Conclusion

We proposed a new pixel employing polarity balanced driving scheme to suppress the degradation of a-Si:H TFT caused by an electrical bias. The proposed circuit, which is based on negative bias annealing, can recover the characteristics of degraded TFT and is verified by circuit simulation with parameters extracted from measured results.

References

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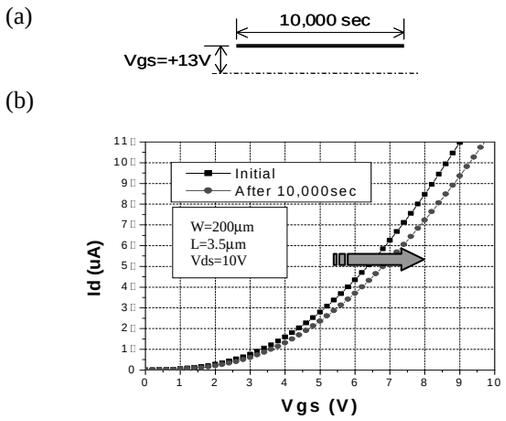

Fig. 1. Continuous bias (a) and measured transfer characteristics (b) (stress condition: t=10,000s, Vgs=13V, Vds=13V)

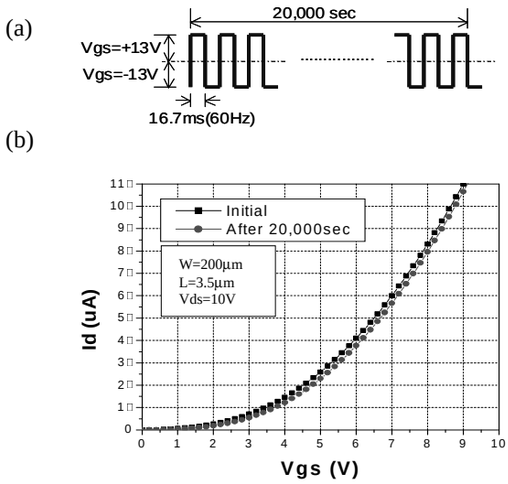

Fig. 2. Polarity balanced biasing (a) and measured transfer characteristics (b) (stress condition: t=20,000s; effective stress time duration =10,000s, Vgs=+13V/-13V duty 50%, Vds=13V)

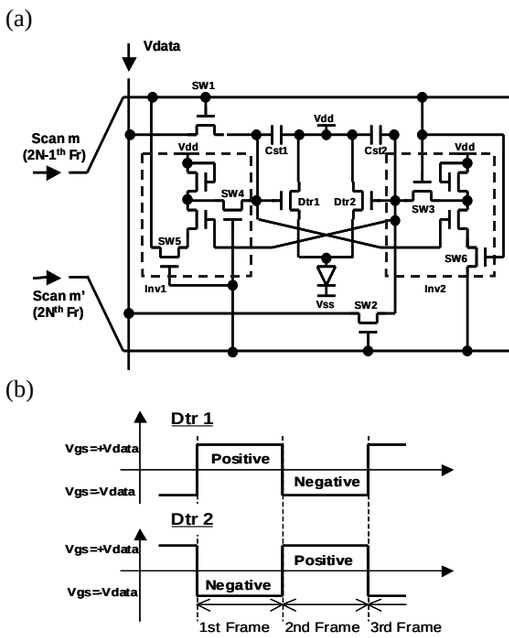

Fig. 3. Equivalent pixel circuit associated with Polarity Balanced Driving (a) and operation sequence (b)