ORGANIC THIN FILM TRANSISTORS OF POLYMER GATE INSULATORS USING DOWNWARD LOW-PRESSURE ORGANIC VAPOR DEPOSITION

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In recent years, thin film transistor (TFTs) based on organic materials as active layer have received considerable interest. Organic TFTs offer advantages compared to traditional field-effect transistors, like mechanical flexibility and weight reduction. Pentacene, a polyacene, consists of five linear benzene rings and has demonstrated the highest electron and hole mobility of organic small molecules. The material exhibits a strong tendency to form highly ordered films which depend on the growth conditions and the substrate. Pentacene thin film have been fabricated by solution precipitation, organic molecular beam deposition, vacuum thermal evaporation, organic vapor phase deposition, all having compared performance. In this work, we have grown the pentacene thin film with new deposition technique such as downward low-pressure organic vapor deposition (DLP-OVD). DLP-OVD proceeds by the sublimed source materials into hot inert gas flow that transports the vapors toward a substrate where condensation of the organic occurs. Opposite the substrate in the reactor, the gas inlet is configured as showerhead from in one surface.

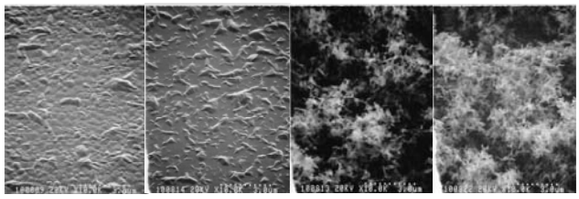
Figure 1 shows the morphology of a pentacene thin film on polymer gate dielectric at various deposition pressures. The deposition time was 30 minutes. Below 10 Torr, the pentacene thin film is formed the continuous thin film. But, above 10 Torr, the pentacene thin film is not formed the continuous thin film. The grain size of the pentacene thin film increases with pressure.

Figure 2 shows the XRD pattern of a pentacene thin film on polymer gate dielectric at various deposition pressures. The peaks arise from the well-known bulk and thin film phases of pentacene. The thin film phase has an interplanar spacing of 15.4 Å, while the bulk-phase has an interplanar spacing of 14.5 Å. At 1 Torr, the pentacene thin film consists of mixture phase and is dominant thin film phase.. However, above 10 Torr, the increase of deposition pressure leads to an amorphous phase.

Figure 3 shows the morphology of a pentacene thin film on polymer gate dielectric at various deposition temperatures. The deposition time was 30 minutes. At 80 ^{o}C, the pentacene thin film is not formed the continuous thin film. The grain size of the pentacene thin film increases with deposition temperature.

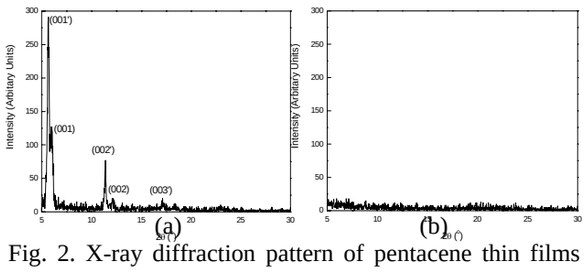
A typical plot of drain current, I_D, vs drain voltage, V_D at various gate voltages, V_G, is shown in figure 4. The mobility and on/off current ratio of pentacene thin films on polymer gate dielectric were 0.12 cm^2/Vs and 10^5, respectively.

In this study, we have grown the pentacene thin film with new deposition technique such as DLP-OVD. Deposition of pentacene thin film using DLP-OVD process is promising deposition technique. Using this method, the pentacene thin film transistors are fabricated on 5 inch wafer.



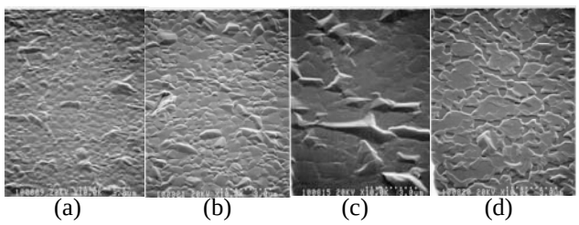
(a) (b) (c) (d)

Fig. 1. Scanning electron micrographs of pentacene thin films deposited by DLP-OVD on polymer gate dielectric at (a) 1 Torr, (b) 5 Torr, (c) 10 Torr, and (d) 30 Torr.



(a) (b)

Fig. 2. X-ray diffraction pattern of pentacene thin films deposited by DLP-OVD on polymer gate dielectric at (a) 1 Torr and (b) 10 Torr.



(a) (b) (c) (d)

Fig. 3. Scanning electron micrographs of pentacene thin films deposited by DLP-OVD on polymer gate dielectric at (a) 0 ^{o}C, (b) 40 ^{o}C, (c) 60 ^{o}C, and (d) 80 ^{o}C.

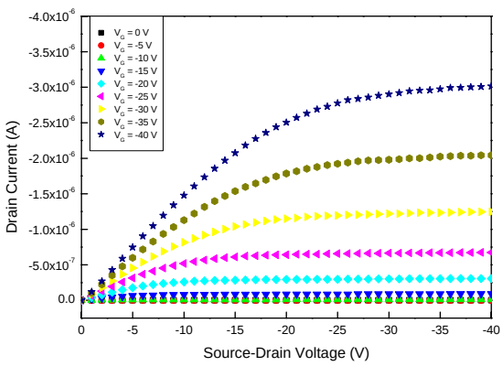


Fig. 4. Plot of drain current vs drain voltage at various gate voltage value on polymer gate dielectric.