Impact of STI width and spacing on the stress generation in deep submicron CMOS

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Introduction. The scaling of the feature size in ultra-large scale integrated (ULSI) technologies necessitates the implementation of advanced isolation schemes. Shallow trench isolation (STI) is the only viable approach for technologies with sub-quarter micron feature size. In order to achieve a higher packing density, STI has to be scaled-down along with a reduction of the device dimensions, generally resulting in increased mechanical stress, related to the oxidation of the sidewalls and corner rounding effects. The stress may affect the electrical device performance, like diode junction leakage and junction capacitance, in different ways. At the same time, the short channel behaviour may be compromised, due to the STI stress impact on the channel and well doping concentration [1]. Therefore, the aim of the paper is to use p-n junction diodes as a tool for the assessment of the p-well doping concentration, for process splits with STI dimensions, corresponding to different CMOS technology nodes. This is achieved by combining current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics.

Experimental. Different geometry shallow n^+-p diodes compatible with deep submicron CMOS HDD junctions have been processed on 200 mm p-type substrates. A shallow trench isolation (STI) depth of 400 nm or 250 nm was used. A retrograde p-well was obtained by a different deep ($1.2x10^{13}$ cm^{-2} @ 180 keV (P0.18) or $1.2x10^{13}$ cm^{-2} @ 120 keV (P0.09)) and a shallow ($1.5x10^{13}$ cm^{-2} @ 55 keV) boron ion implantation, followed by a dopant activation anneal (10 min, 850 ^oC). The n^+ region was created by an arsenic ion implantation ($4x10^{15}$ cm^{-2} @ 50 keV) and anneal (10 s 1100 ^oC). This was followed by Co-silicidation with a titanium cap layer (12/8 or 10/8) with a maximum temperature annealing of 850 ^oC. The thermal budget T0.18 is considered higher than T0.09. A description of the split batch diodes is given in Table I.

The static *I-V* characteristics of the diodes were measured on wafer level, in the dark, and in the range of –1 V to 2 V. The bias was applied to the back p-type substrate and the current was measured at the grounded top n^+ and bottom contact. Further, *C-V* characteristics have been measured on the same diodes at a frequency of 100 kHz, in order to assess the doping density and profile and the depletion width. The latter parameter can be used to transform the reverse bias axis into a depth axis, so that one can easily obtain profiles of the electrical parameters.

Results and discussion. First, the STI layout dependence of the capacitance will be investigated for different process splits. It is observed that the capacitance is dominated by the area component. At the same time, the capacitance is strongly dependent on the active area width and trench spacing. A higher capacitance is found for a smaller active area width, in the range 0.2 to 3 μm, while the capacitance also increases for a larger trench width. Such an increase in C can result either from a reduction of the built-in potential, i.e., by an STI stress-induced reduction of the silicon band gap or from an increase in the p-well doping density N_{well}.

A systematic study has pointed out that the capacitance variation is mainly due to a change in N_{well} [2]. The resulting doping profiles for the splits of Table I are shown in Fig. 1. A higher active doping concentration is observed in P0.09 than P0.18, which is due to the lower implantation energy. The highest active doping concentration in this study is found for the shallowest STI depth. It also follows from Fig. 1 that the doping profile depends on the thermal budget, while the different silicide thickness has only a marginal impact.

These results will be discussed in view of the STI related stress and its influence on the diffusion of dopants (i.e., B) [1]. This is an important result since a further down-scaling is needed to precisely control the doping concentration while the stress is expected to increase for smaller and shallower STI.

References

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Table I. Description of the split batch diodes for investigating the p-well doping concentration, corresponding with different processing conditions.

Wafers	Trench Depth (nm)	I/I condition	Thermal budget	Silicide
D04	400	P0.18	T0.18	12/8
D11	400	P0.09	T0.18	12/8
D13	400	P0.09	T0.18	10/8
D18	250	P0.09	T0.18	12/8
D22	250	P0.09	T0.09	10/8

Fig. 1. Active doping concentration versus depletion width of 0.2 μm active area width and 0.3 μm active area spacing for different wafers.