# TRACE METAL CONTAMINATION ANALYSIS OF THE BEVEL AND EDGE EXCLUSION AREA ON STARTING SILICON

Chris M. Sparks and Meredith R. Beebe
International SEMATECH
2706 Montopolis Drive, Austin, Texas 78741 USA

The edge exclusion area of the silicon wafer has become increasingly relevant as it is pushed towards becoming a smaller region in order to provide more surface area for device manufacturing. Contamination from the edge or bevel of a wafer is important to monitor as it could affect device yield due to diffusion of the metals to critical regions of the wafer or it could cross contaminate other wafers in the manufacturing line. Pathways that contribute to cross contamination of the edge of the wafer would include edge grip wafer handling, centering pins for wafer alignment, and the FOUPs or cassettes the wafers rest on.

Historically, it has been difficult to quantify trace metal contamination in the edge exclusion area of wafers with the traditional analytical toolset. At International SEMATECH we have developed a technique known as the beveled edge analysis tool (BEAT) to precisely sample the edge exclusion region for quantification of trace metals [Figure 1]. We shown good correlation between the BEAT technique and other analytical methods (for example, total reflection x-ray fluorescence spectroscopy and vapor phase decomposition inductively coupled plasma mass spectrometry) on uniformly contaminated wafers. Details of the development of the BEAT technique and qualification experiments can be found in [1].

Previous experiments with test quality wafers have shown that there is trace copper contamination on that class of starting silicon [1, 2]. This presentation will focus on the analysis of new production quality polished and epitaxial silicon wafers from various wafer suppliers. We will also be looking beyond copper for an expanded list of metal contamination. Trace metal data from the wafer suppliers will be anonymously compared and contrasted.

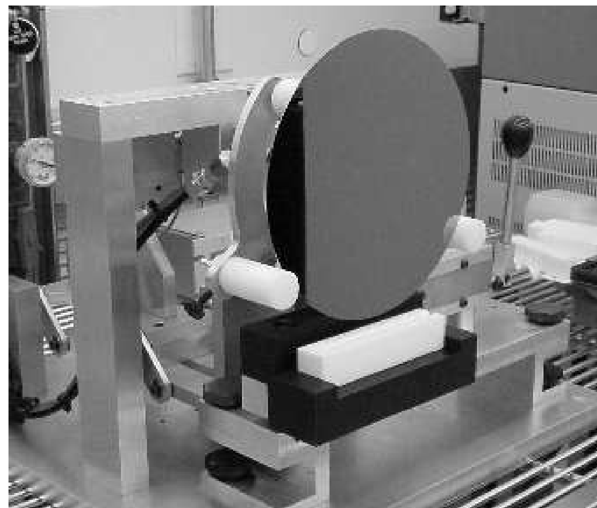

Figure 1. BEAT apparatus holding a 200mm wafer prior to analysis.

References:

1. C. Sparks, C. Gondran, P. Lysaght, and J. Donahue. “Novel Technique for Contamination Analysis around the Bevel and Edge Exclusion Areas of 200 and 300mm Silicon Wafers.” *Process and Materials Characterization and Diagnostics in IC Manufacturing, Proceedings of SPIE,* Vol. 5041, 99, 2003.

2. M. Beebe, C. Sparks, and R. Carpio. “Should We Analyze for Trace Metal Contamination at the Bevel and Edge Exclusion of Silicon Wafers?” *Characterization and Metrology for ULSI Technology: 2003 International Conference*, Edited by D. Seiler, et al., 309.