

High Deposition Rate Cu Plating for Pillar Bump Application

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Emerging higher density, faster speed, and lower-cost flip-chip packaging demands more critical processing than the previous generation of flip-chip devices. Pillar-bumped flip-chip packages provide superior electrical and thermal enhancement and a lower profile ⁽¹⁾. The copper pillar's high standoff of about 100 microns enables better flow for the over mold compound. In order to meet high through-put demands, electrodeposition of 50 to 100 micron thick of Cu pillars is a challenge for wafer electroplating processes.

Three length scales of uniformity, i.e. bump (micrometers), die (millimeters), and wafer (tens of centimeters), are typically considered in bumping processes ⁽²⁾. The uniformity within a die is determined mostly by the within-die pattern and the size of the spaces between die combined with the plating chemistry and deposition rate. Wafer scale uniformity is primarily governed by the process cell architecture, deposition rate, and plating chemistry.

A uniform and thin boundary layer may be created using a shear plate agitation mechanism ⁽³⁾. Results are discussed showing that pulse current waveform in combination with thin and uniform boundary layer fluid flow improves the copper column uniformity at high deposition rates.

Figure 1 shows the effect of current wave form combined with thin boundary layer on the within die uniformity at a deposition rate of 5.0 $\mu\text{m}/\text{min}$. Figure 2 shows the effect on within die uniformity at relative low deposition rate up to 1.5 $\mu\text{m}/\text{min}$.

Reference

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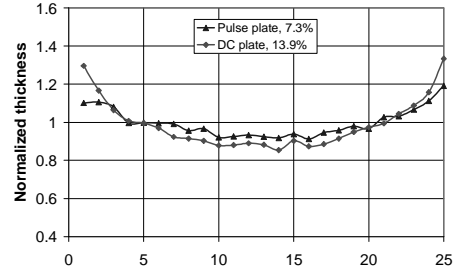


Figure 1. Effect of current wave form on within wafer uniformity (one sigma) at deposition rate of 5 $\mu\text{m}/\text{min}$.

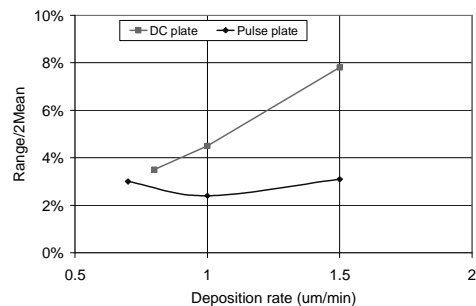


Figure 2. Effect of current density on the within die uniformity at relative low deposition rate