Advancement Of Technology Elements In Recent Build-up Substrate

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The “Build-up PCB” has emerged in 1990 and expanded the application in wide spectrum from mobile phone to super computer in the last decade.

Build-up PCB substrate

Fig.1 shows a cross section of lines formed by pattern plating. 20µm line/space is the most advanced production capability for ASIC substrate. The thickness of electro-less plating has to be low in contrary with a requirement as an enough current base in electro plating. Also, the surface anchor depth is expected to be low as possible due to interference to a skin effect.

After line width and pitch are defined dielectric thickness is determined. If the line width is 30µm, the dielectric height is 35µm in strip line construction to set characteristics impedance with 50 ohms. When a dielectric height is defined, a dimension of via hole is defined to 50µm with maintaining an aspect ratio of via hole under 0.7 so that the hole is plated smoothly. UV-YAG laser can effectively drill a small diameter below 50µm than CO_2 due to short wave length.

Flip chip joint pad

Structures of flip chip joint pad on build-up PCB substrate are shown in Fig.2 as “Solder Mask Defined” and “Non Solder Mask Defined”. NSMD has a large advantage in chip placement process since the edge of solder mask does not obstruct the chip bump to sit in the solder mask opening. However, as shown in the figure, overall height is low compared with SMD if joint solder volume is the same. Both types can meet reliability requirement.

Electrical performance

According to the signal attenuation simulation, chip-to-chip communication with variation of package type is assessed. The critical clock length is calculated according to the package type and chip dimension. Fig.3 shows the result of simulation. With considering the limit of attenuation, a comparison is shown with 10GHz signal speed. It is obvious that signal attenuation and delay are degraded with the package size increase that makes a critical clock length longer.

Future requirement

In ITRS2003, area array flip chip pitch will not be expected to follow the reduction predicted in 2002 issue. In the meantime, peripheral flip chip joint is struggling to increase I/O’s since it is not allowed to place joint in active circuit area due to compression bonding to a chip terminal. An emergence of ultra fine pitch area array technology with low cost mean is highly desired.

SUMMARY

-Build-up wiring reached to 20µm/20µm line/space with employing 50µm diameter micro-via hole drilled by UV-YAG laser.

-Overall system performance depends on package type. Bare chip SiP is the best, particularly in double side attach.

-Fine pitch area array with employing hard metal in joint is expected digital consumer products.

REFERENCE

[1]http://public.itrs.net/Files/2001ITRS/Home.htm

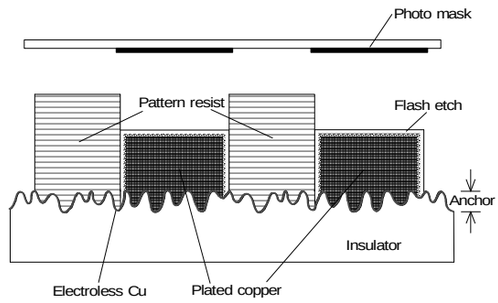

Fig.1 Cross section of lines

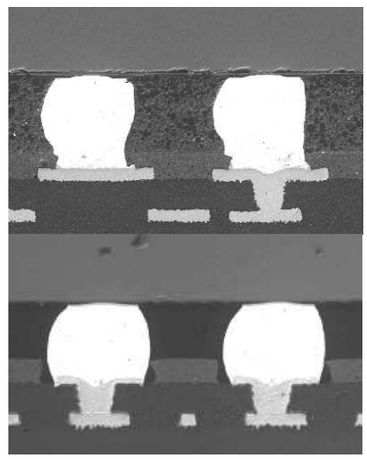

Fig.2 SMD and NON-SMD joint

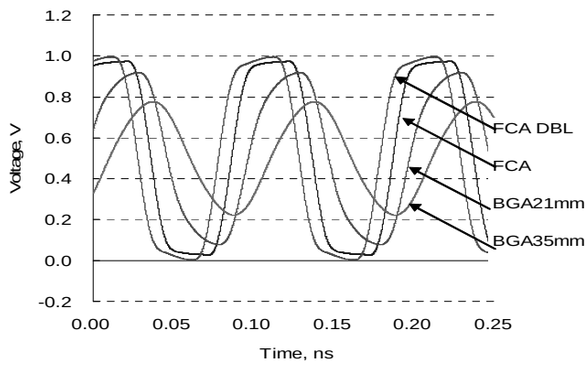

Fig.3 Signal delay in 10GHz